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Comparative study of the design and simulation of an AC to high DC voltage generation circuit

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Abstract

Decades after the invention of the Cockcroft–Walton voltage multiplier, it is still being used in broad range of high voltage and ac to dc applications. High voltage ratio and high efficiency are its main features. Due to the limitations of original circuit, reducing the output ripple and increasing the accessible voltage level motivated scientists to propose new topologies. However, over the worldwide bibliography, most of Cockcroft-Walton voltage designers persist in using equal capacitances in every stage without considering an optimal design. The aim of this paper is to do a comparative study of the design and simulation of a fixed model (conventional model used by most authors) and a variable model (new design) of generating High Voltage Direct Current (HVDC) based on Cockcroft–Walton voltage multiplier that stresses on the choice of the adequate capacitance values to reduce the output voltage drop, produce less ripple and the calculations of the optimal number of stages that is necessary to produce the desired output voltage with a better performance. The generation of HVDC based on Cockcroft–Walton voltage multiplier and an eight stage was used for simulations and theoretical analysis which yielded up to 4.4 kV DC from an input voltage of 230 V, 50 Hz ac supply. The results are compiled from the simulations done on MATLAB/SIMULINK, by the designs and simulations characteristics of the models the performances, output voltages and ripple voltages per stage have been compared.

Keywords: Cockcroft–Walton voltage multiplier, HVDC, Capacitance, Performance

Introduction

In this modern world, HVDC system provides a secure and stable asynchronous interconnection of power grids that operate on different frequencies. In addition, HVDC provides instant and precise control of power flow. HVDC transmission is becoming more popular in the present scenario of bulk power transmission over long-distances, it is necessary to study the testing of various insulation materials. To get HVDC output from a smaller input voltage many methods have been utilized to perform this task. Some of the most common methods used to produce a voltage larger than the power supply voltage are step-up transformers [1], voltage doublers [2, 3], multiplier circuits [4–6], charge pump circuits [7], switched-capacitor circuits [8] and boost or step-up converters [9]. High voltage conversion ratio is becoming increasingly essential in a multitude

of industrial and laboratory research applications [10, 11], such as front-end stages for batteries or photovoltaic sources, DC backup systems, UPS devices, step down inverters and many more. Voltage Multipliers and especially the half-wave Cockcroft–Walton voltage multiplier are at the forefront of these applications and methods [12–14]. The diode capacitor topologies are more suitable [15]. In 1920 Greinacher, a young physicist published a circuit [16] which was improved in 1932 by a British physicists John Douglas Cockcroft and Irish physicists Ernest Thomas Sinton Walton to produce high-energy positive ions [17]. Cockcroft and Walton invented the Cockcroft-Walton voltage multiplier (CWVM).

Cockcroft–Walton voltage multiplier

Voltage multiplier circuits are primarily used to develop high voltages where low current is required. The output voltage of voltage multiplier circuits may be several times more than the input voltage. For this reason, voltage multipliers are used in special applications where load is constant and has high impedance or where the stability of the input voltage is not critical. The advancement in studies focus on different hardware circuits that can offer high voltage conversion ratio, small output voltage ripple, high efficiency, simple design and low cost. Among these, the Half Wave CWVM is highly used as AC to DC convertor [18]. A half wave voltage doubler is shown in Fig. 1.

During the first half of the supply period, diode D_1 is turned on and diode D_2 is turned off, capacitor C_1 is being charged to the peak value of input voltage. During the second half cycle, diode D_2 is turned on and diode D_1 is turned off, charging capacitor C_2 to the twice the peak value of input voltage because capacitor C_1 (charged to Vs) and input voltage (Vs) now act as series aiding voltage source. When input voltage returns to its original polarity, diode D_2 is again reverse biased (off), and then the capacitor C_2 will be discharged through the load R. The time constant RC_2 is so adjusted that C_2 has little time to lose any of its charge before the input polarity reverses again. During the negative half cycle, diode D_2 is turned on, capacitor C_2 will be recharged again until voltage

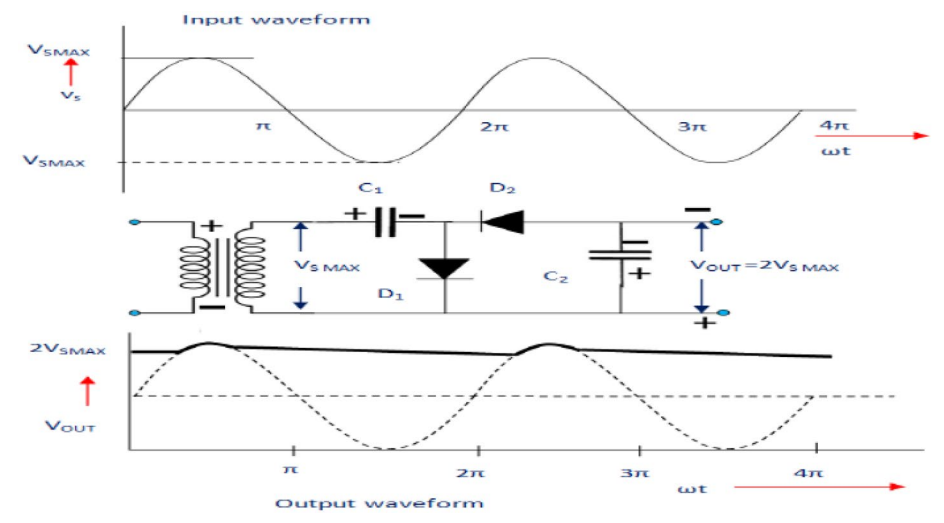

Fig. 1 Half wave voltage doubler [19]

across it is again equal to 2Vs. Cockcroft-Walton Voltage value increases as it goes through each stage of the voltage multiplier. Multipliers are made up of multiple stages, they may be classified as voltage doublers, triplers, quadruplers, etc. The classification depends on the ratio between the output voltage and the input voltage.

Design of the multiplier circuit

Diode selection

Diode at each level of the voltage multiplier performs two major operations as firstly, it conducts to discharge every capacitor at each level and secondly it blocks the reverse voltage to prevent the unwanted conduction [20]. To choose our diode the following basic device parameter must be considered.

- **Repetitive peak reverse voltage**

Multiplier circuit reverse voltage seen by each diode is 2Vm in Cockcroft-Walton voltage multiplier. So, the device must be selected with reverse voltage (VRRM) setting of at least 2Vm. Therefore, we have to select the diode voltage rating 2Vmax for the safety purpose [4].

- **Frequency of input signal**

While selecting the diodes for the rectifier, the frequency of input voltage to the multiplier circuit must be considered. For symmetrical input signals, the device chosen must be capable of switching at speed faster than the rise and fall times of the input [21]. If the reverse recovery time is too long, the efficiency and regulation of the device will be affected. In the worst-case insufficient recovery speed will result in accessing heating of device. In this case, the device will be permanently damaged. The reverse recovery time is conditioned by the circuit and the conditions used to make the measurement. Reverse recovery Time specification should be used for qualitative, not quantitative purposes since condition specified for the measurement rarely reflects those found in actual real life circuit operation [4]. Decreasing current flow in the multiplier circuit allows higher input frequency to be used. An increase in current flow has been the opposite effect. Ideally, the network load multiplier should draw no current.

- **Peak forward surge current (Ifsm)**

Most rectifier diodes have a peak forward surge current rating. This value (rating) corresponds to the maximum peak value of single sinusoidal half-wave which, when superimposed on the nominal load current of the device, can be conducted without damaging of rectifier. This value becomes important when considering the large capacitance associated with multiplier network. Due to the capacitive loading effects on the rectifier, surge currents can be produced. With a high step-up turn ratio of the transformer, capacitor C_1 on the secondary side is considered to be the largest one. Its value can be determined as follows:

$$C_1' = NC_1 \tag{1}$$

Where; C_1 = first multiplier circuit capacitance,

C_1' = Referred capacitance on primary side

$N =$ turns ratio of high voltage transformer $\frac{N_2}{N_1}$.

When the circuit is turned on, large current develops in the primary side as this effective capacitance begins to charge. On the secondary side, large surge current can flow through the rectifiers during initial capacitor charging at turn on. The addition of a series resistance Rs can greatly reduce these current surges as well as those in the primary circuitry.

$$Rs = {}^{V_{\text{Peak}}}/_{Ifsm} \tag{2}$$

- **Forward current (I_O)**

In ideal multiplier circuits, the load will draw no current. Ideally, large current flow through the rectifier occurs during capacitor charging. Therefore, device with very low current rating (100 mA) and in case of cables. Micro amperes are also used. It must be noted that forward current and forward surge current rating are related [4]. Both are the function of silicon die area. It is truly speaking that device with a high surge current rating I_{fsm} will also have high forward current I_O rating and vice versa.

- **Forward voltage (V_f)**

In practice the forward voltage drops V_f of the rectifier does not have a significant effect on multiplier networks on the overall efficiency [4]. The calculation of the voltage drop is given by Eq. (3). For a half wave doubler (two stages) multiplier having an output voltage of 8000 V, and considering a forward voltage drop of the rectifier diodes as 2 V (for a forward current of 100 mA), its voltage drop is 0.05%.

$$\text{Voltage drop} = \text{No. of stages} * \left({}^{\text{Forward voltage}}/_{\text{Output voltage in V}}\right) * 100 \tag{3}$$

Capacitor selection

The size of capacitors used in multiplier circuit is proportional to the frequency of input signal. Capacitor used in off line, 50 Hz application is typically in the range of 1.0 to 200 microfarad. The rated voltage of capacitor is determined by the type of multiplier circuit. The capacitor must be able to withstand a maximum voltage depending upon the numbers of staged used. A good thumb rule is to choose capacitor whose voltage rating is approximately twice that of actual peak applied voltage. Due to the AC impedance of the capacitors, there is a voltage drop V_{drop} and a peak-to-peak voltage ripple δV when the circuit is loaded [22–24]. Based on the theoretical analysis and the assumption presented in [22, 25, 26], the ratio X of the output voltage V_{out} over V_{max} the maximum value of the sinusoidal input supply voltage, is given by the equations;

$$\frac{V_{\text{out}}}{V_{\text{max}}} = X = X_{nl} - \frac{1}{V_{\text{max}}}\left(V_{\text{drop}} + \frac{1}{2}\delta V\right) \tag{4}$$

$$X_{nl} = \frac{V_{\text{out},nl}}{V_{\max}} = 2n \tag{5}$$

$$\frac{V_{\text{out}}}{V_{\max}} = \frac{g}{f}\left(\sum_{i=1}^{n}\frac{(n+1-i)^2}{C_{2i-1}} + \sum_{i=1}^{n-1}\frac{(n+1-1)(n-1)}{C_{2i}}\right) \tag{6}$$

$$\frac{\delta V}{V_{max}} = \frac{g}{f}\sum_{i=1}^{n}\frac{(n+1-i)}{C_{2i}} \tag{7}$$

where X_{nl} is the no-load voltage ratio,n the number of stages, f the frequency of the voltage supply, I_l the average value of the load current and

$$g = \frac{I_l}{V_{\max}} \tag{8}$$

For the Fixed selection of capacitors;

$$C_{2i} = C_{2i-1} = C \tag{9}$$

and for the Variable selection of capacitors

$$C_{2i} = C_{2i-1} = (n+1-i)C \tag{10}$$

where i is the number of every stage and C the capacitance of the last stage (base capacitance). Considering that the total capacitance C_{tot} is the sum of all the capacitances of each topology

$$C_{\text{tot}} = \sum_{i=1}^{n} C_i \tag{11}$$

Voltage gain for the two models can be calculated as a function of C_{tot}.

$$\text{Fixed model} : X = 2n - \left(\frac{g}{f \times C_{\text{tot}}} \times \frac{n\left(8n^3 + 9n^2 + n\right)}{6}\right) \tag{12}$$

$$\text{And } C_{\text{tot}} = 2nC \tag{13}$$

$$\text{Variable model} : X = 2n - \left(\frac{g}{f \times C_{\text{tot}}} \times \frac{n^2(n+1)(2n+1)}{2}\right) \tag{14}$$

$$\text{And } C_{\text{tot}} = n(n+1)C \tag{15}$$

Figure 2 provides information of the gain $X = \frac{V_{\text{out}}}{V_{\max}}$ of the Fixed and Variable model against the number of stages for a fixed value of $\frac{g}{f \times C_{\text{tot}}}$.

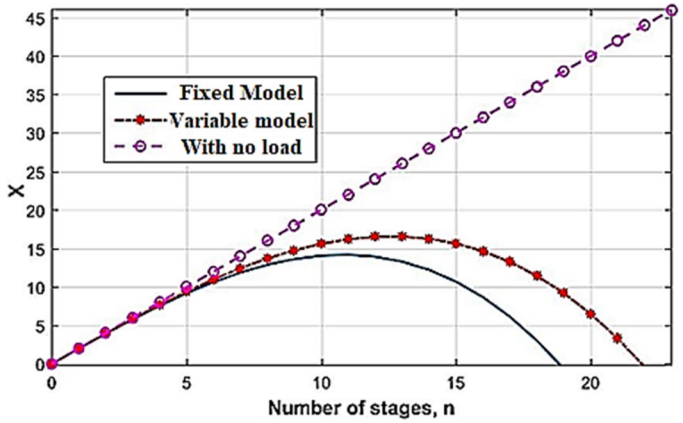

Fig. 2 The gain X as a function of the Number of stages, n for the different models

Selection of number of stages

- **Fixed model selection of number of stages**

The selection of the number of stages in a Cockcroft Walton voltage multiplier circuit depends the desired output level. For fixed values of capacitances in the various stages, the number of stages should be in accordance with the required output voltage and the voltage drop till last stage [27]. The equation to calculate the number of stages is as follows:

$$n = \frac{V_{\text{out}} + V_{\text{drop}}}{2 \times V_{\text{peak}}} \tag{16}$$

where;

$n =$ Number of stages

$V_{\text{out}} =$ Output Voltage

$V_{\text{drop}} =$ Voltage drop till last stage

$V_{\text{peak}} =$ Input peak voltage

If we gets the value in fraction in the above equation then consider the nearest greater integer for the selection of the number of stages.

- **Variable model selection of number of stages**

Cockcroft-Walton output voltage as a function of number of stages n, peak input voltage V_{max}, output current I_l, and product fc of frequency f and capacitance c [23].

$$V_{\text{out}} = 2nV_{\text{max}} - V_{\text{drop}} \tag{17}$$

$$V_{\text{drop}} = \frac{I_l}{6fc}\left(4n^3 + 3n^2 - n\right) \tag{18}$$

$$V_{\text{out}} = 2nV_{\max} - \frac{I_l}{6fc}\left(4n^3 + 3n^2 - n\right) \tag{19}$$

From the V_{out} expression, due to the fast growth of the n^3 term in the negative term (voltage drop relative to the no-load value), if n starts from zero and increases without changing other parameters, V_{out} first increases, then reaches a peak, and then decreases [28]. The derivative of V_{out} with respect to n is zero at peak V_{out} deriving the optimum number of stages (Fig. 3).

$$n_{\text{opt}} = \frac{1}{8V_{\max}}(-V_{\max} + 2V_{\text{out}} + 2(V_{\max} + 2V_{\text{out}})\cos \left[\frac{1}{3}Arc\text{Tan}\left[\frac{4V_{\max}\sqrt{V_{\text{out}}(2V_{\max} + V_{\text{out}})}(-V_{\max} + 2V_{\text{out}})(V_{\max} + 14V_{\text{out}})}{-V_{\max}^3 - 22V_{\max}^2 V_{\text{out}} + 12V_{\max}V_{\text{out}}^2 + 8V_{\text{out}}^3}\right]\right]\Bigg) \tag{20}$$

Optimum n depends on input and output voltages $V_{\max}$, and V_{out} only, not on output current nor frequency or capacitance. Knowing the ratio of V_{out} to $V_{\max}$ which is X, n_{opt} can further be simplified as:

$$n_{\text{opt}} = \frac{1}{8}\left(-1 + 2X + (2 + 4X)cos\left[\frac{1}{3}ArcTan\left[\frac{4\sqrt{X(2+X)(-1+2X)(1+14X)}}{-1+2X(-11+6X+6X^2}\right]\right]\right) \tag{21}$$

Ripple factor and ripple voltage

- **Ripple voltage for Fixed model**

Ripple of the n-stage multiplier for the Fixed model will be [4];

$$2\delta V = q\sum_{n=2}^{2n}\frac{1}{C_n} \tag{22}$$

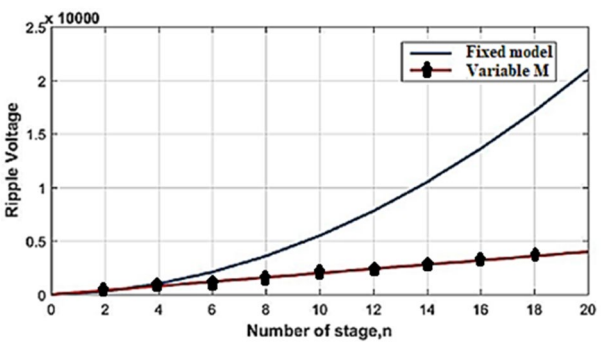

Fig. 3 Variation of Ripple with number of stages in CWVM

$$q = IT \tag{23}$$

$$q = \frac{I}{f} \tag{24}$$

For n stage total ripple is given by;

$$2\delta V = q\left(\frac{1}{C_{2n}} + \frac{2}{C_{2n-2}} + \frac{3}{C_{2n-4}} + \frac{4}{C_{2n-6}} + \ldots + \frac{n}{C_2}\right) \tag{25}$$

For $C_{2n} = C_{2n-2} = C_{2n-4} = C_{2n-6} = \ldots = C_2 = C$

$$\Rightarrow \delta V = \frac{I}{2fC}\left(\frac{n(n+1)}{2}\right) = \frac{I}{fC}\left(\frac{n(n+1)}{4}\right) \tag{26}$$

- **Ripple voltage for Variable model**

Ripple of the n-stage multiplier for the Variable model is given as

$$\delta V = \frac{n \times I_l}{fC} \tag{27}$$

Ripple voltage is the magnitude of fluctuation in DC output voltage at a specific output current (assuming AC input voltage and AC input frequency are constant) [29]. In addition, ripple is function of number of stages and the switching frequency for a fixed capacitor design. Hence, varying frequency ripple can be reduced and can be treated as high frequency switching of CWVM network [30]. For pertaining the same threshold Fig. 4 provides information regarding variation of ripple with respect to the various frequency level.

Voltage drop for fixed and variable model

Generally, in order to reduce the complexity of the circuit equations, the calculation of the diode voltage drop is neglected. Also, parasitic effect of diode and capacitor is

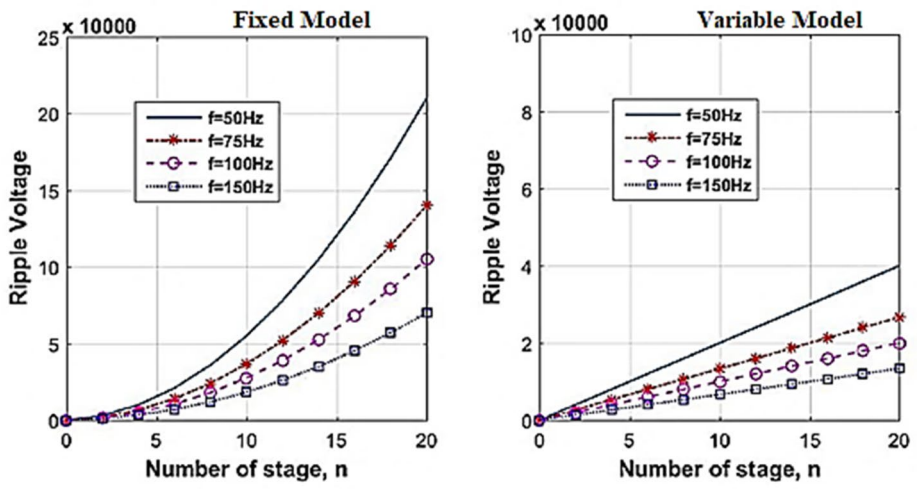

Fig. 4 Ripple Voltage in CWVM against different frequencies

neglected as its contribution is very small in the system. There are two modes of operation of CWVM the no load operation and operation under loaded condition [30]. There is drop due to internal behavior and load applied when the load is connected. This drop (considerably high) reduces the output voltage significantly.

Total drop is:

$$\Delta V = \Delta V_n + \Delta V_{n-1} + \Delta V_{n-2} + \cdots + \Delta V_1 \tag{28}$$

- **For the Fixed model**

On solving for each stage drop, the Fixed model drop gives us [31];

$$\Delta V_2 = \frac{q}{C} n \tag{28a}$$

$$\Delta V_4 = \frac{q}{C}[2n + (n-1)] \tag{28b}$$

$$\Delta V_{2n} = \frac{q}{C}[2n + 2(n-1)] + \cdots + 2 \times 2 + 1] \tag{28c}$$

Adding all n voltage drops gives the total voltage drop on load:

$$\Delta V_{\text{total}} = \frac{q}{C}\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right] \tag{29}$$

$$\Delta V_{\text{total}} = \frac{I}{fC}\left[\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right] \tag{30}$$

- **For the Variable model**

The total voltage drop [23] for the variable model gives us;

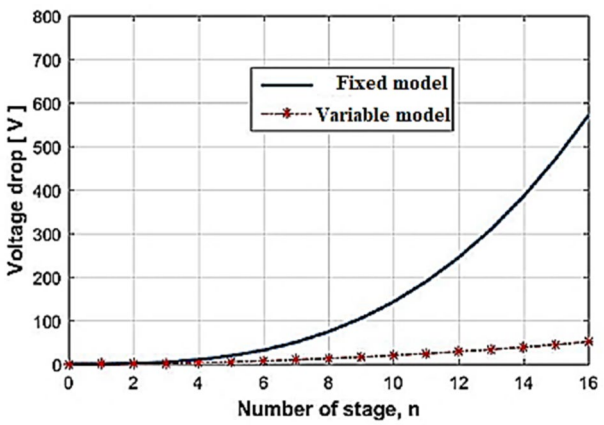

Fig. 5 Variation of Voltage Drop for a fixed frequency

Table 1 Simulation parameters of the HVDC

No	Input voltage	Input frequency	Number of stages, n	Transformer Secondary voltage	Capacitor
1	230 V	50 Hz	8	230 V	$150\mu F$
Fixed Model design					
2	$C_1 = C_2 = C_3 = C_4 = \ldots = C_{15} = 150\mu F$				
Variable Model					
3	$C_1 = C_2 = 1200\mu F$, $C_2 = C_3 = 1050\mu F$, $C_4 = C_5 = 900\mu F$, $C_6 = C_7 = 750\mu F$, $C_8 = C_9 = 600\mu F$, $C_{10} = C_{11} = 450\mu F$, $C_{12} = C_{13} = 300\mu F$, $C_{14} = C_{15} = 150\mu F$,				

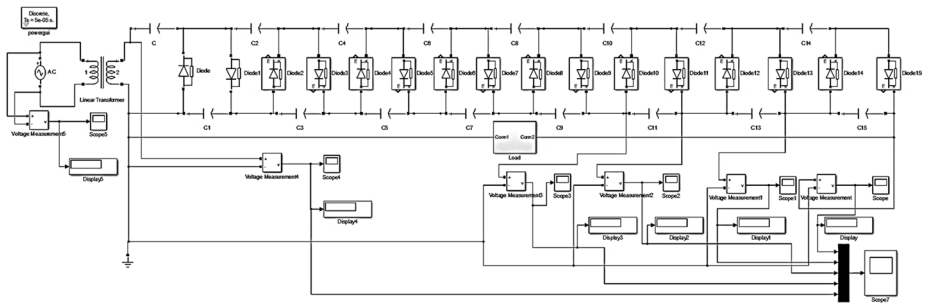

Fig. 6 HVDC Circuit diagram for a single Model

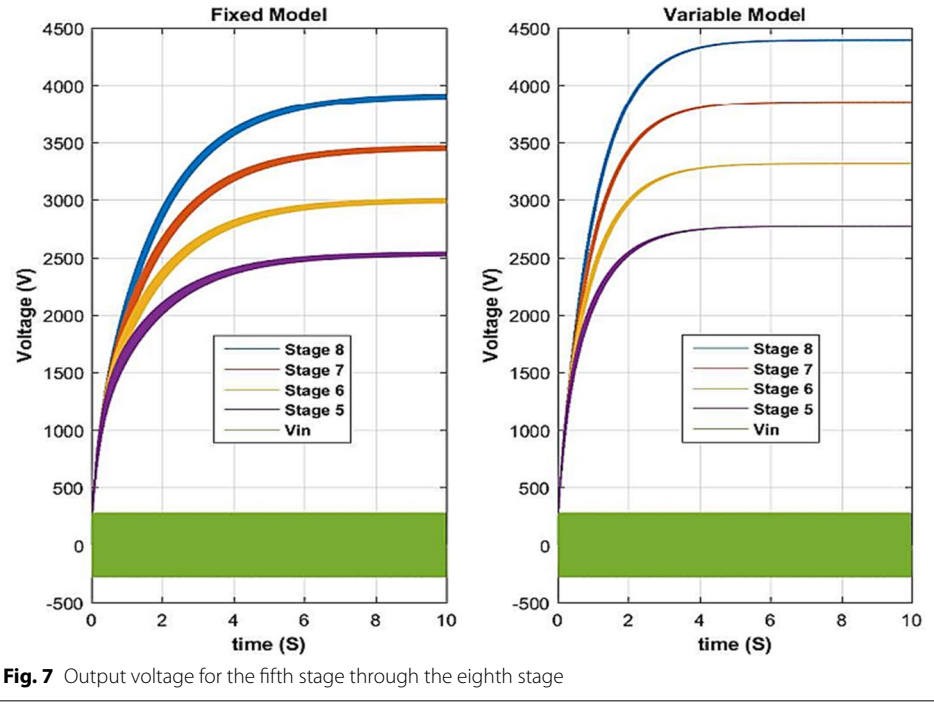

Fig. 7 Output voltage for the fifth stage through the eighth stage

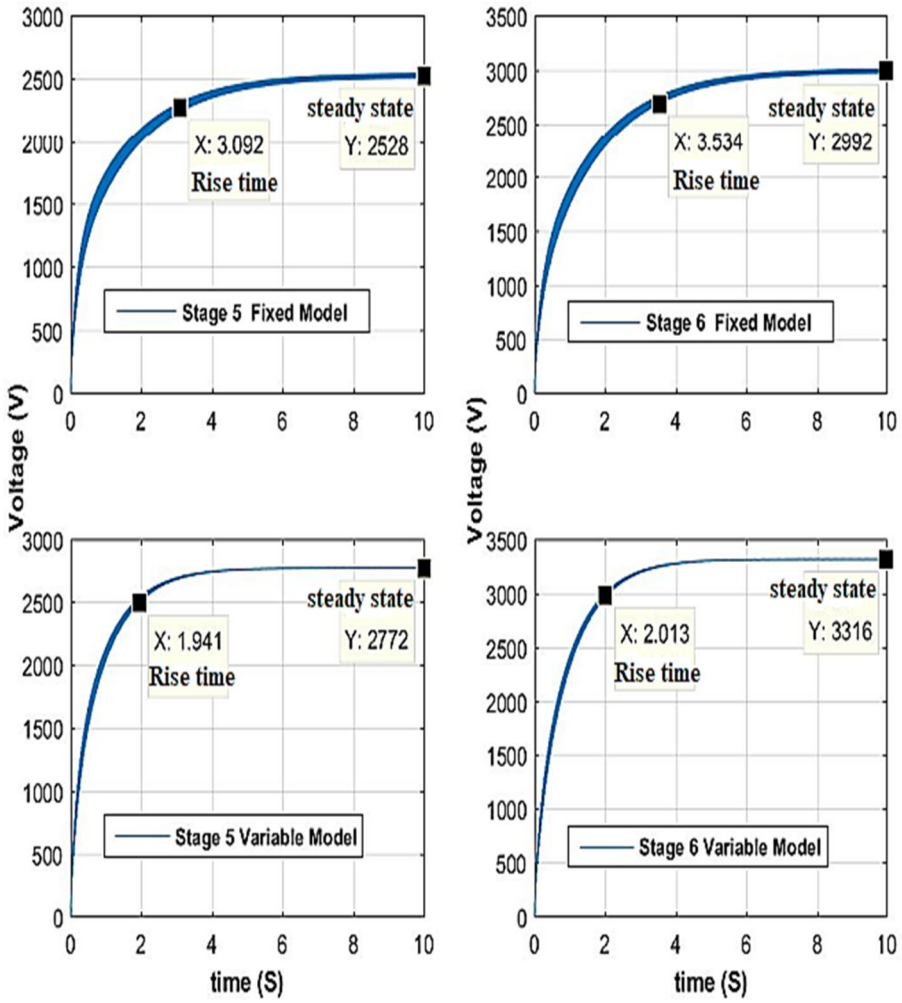

Fig. 8 Rising time, transient and steady state value of output voltage of stages five and six of both models

$$\Delta V_{\text{total}} = \frac{n^2 I}{f \times C} \tag{31}$$

Figure 5 shows us the Variation of Voltage drop against a fixed frequency.

Simulations

The parameters for the simulation are presented in the table below (Table 1):

Circuit diagram

See Fig. 6

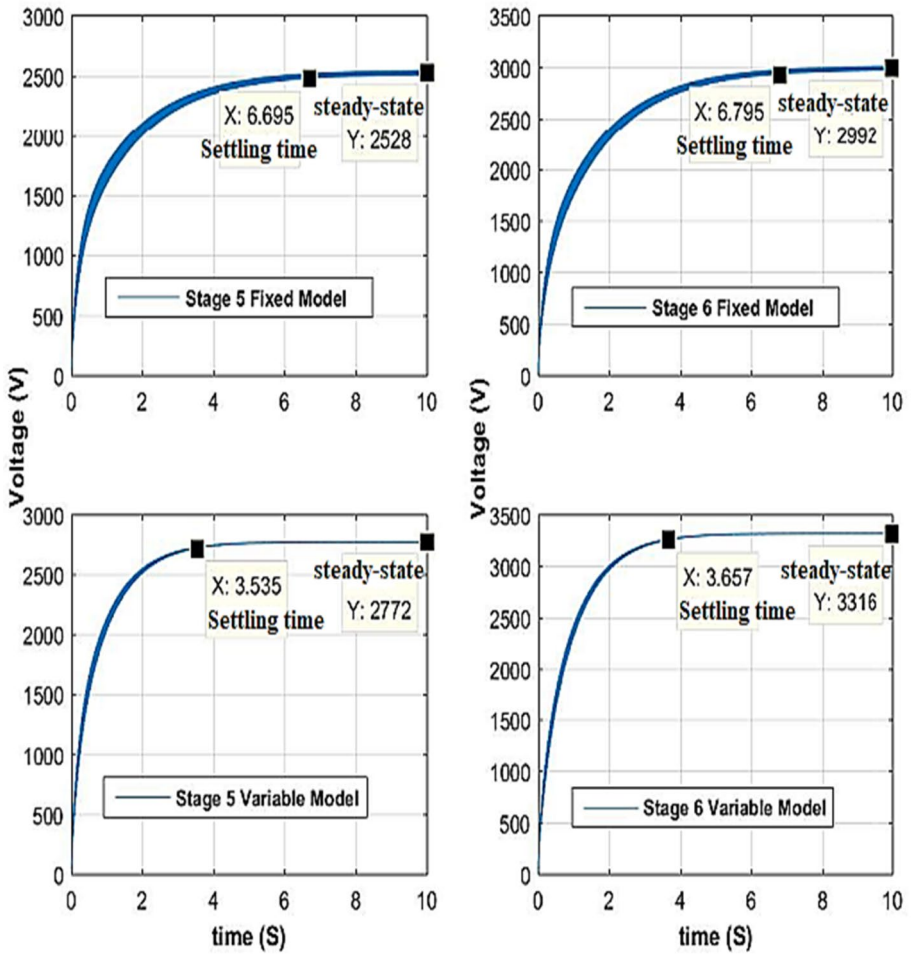

Fig. 9 Settling time, transient and steady state value of output voltage of stages five and six of both models

Comparison of the fixed capacitors model and the variable capacitors model

Here the output voltage, performance and the ripple voltage of both systems will are compared.

- **Output voltage comparison**

From the simulation results show in Fig. 7, it is clear that the output voltage of the Variable capacitors model is greater than that of the fixed capacitors model. From stages 5 to 8, the increase in the output voltage is from 250 to 500 V.

Performance comparison

From the output waveform, the rising and settling times of the fixed capacitors model and the variable capacitors model can be compared below;

From the simulation results and the values. It is clear that the Variable model is more rapid than the fixed model, both models are stable. Therefore, the Variable model is more performant than the fixed model (Figs. 8, 9, 10, 11 and 12).

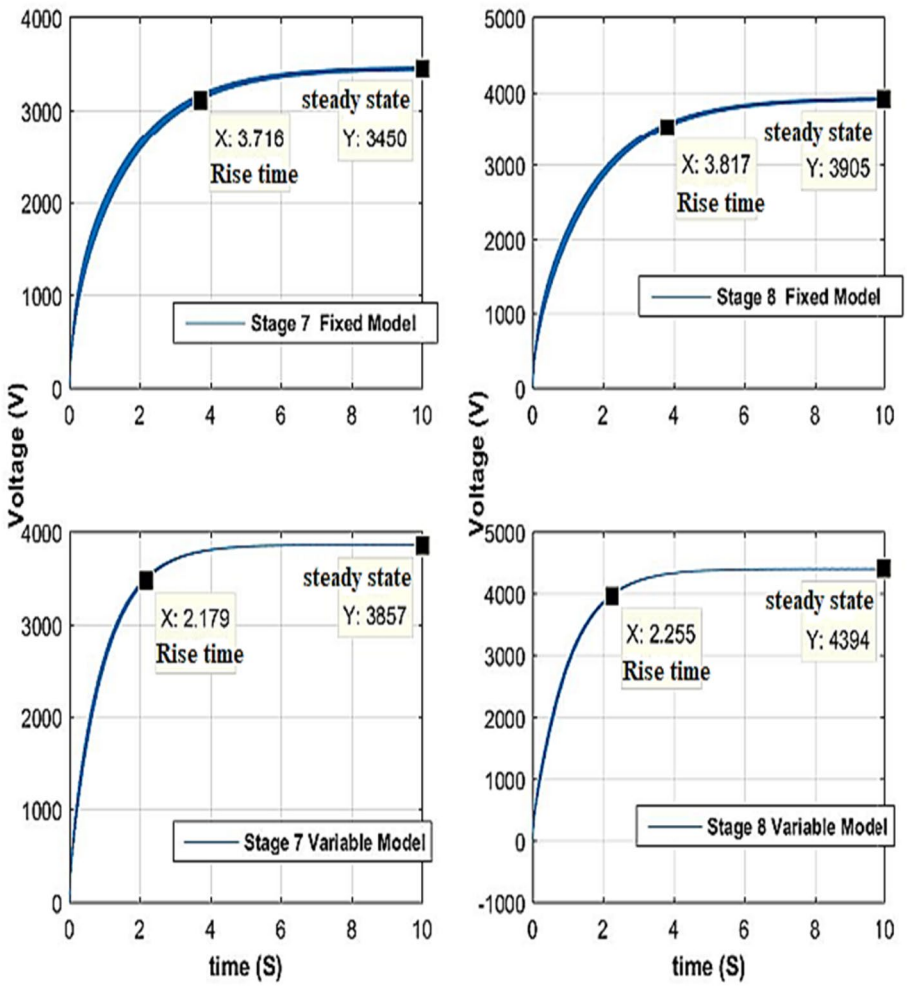

Fig. 10 Rising time, transient and steady state value of output voltage of stage seven and eight of both models

- **Voltage ripple comparison**

From the simulation and the output waveform the voltage ripple of the Fixed and Variable model is presented:

Steady-state ripple of the generated HVDC versus time for stage five through stage eight of both models. From the ripple it is clear that the voltage ripple of the Variable model is lesser than that of the fixed model and for both models the higher the stage there is an increase in the voltage ripple.

Conclusion

In this work, the design and simulation of two methods are presented based on Cockcroft-Walton Voltage multiplier. The output voltage, performance and voltage ripple were compared for the two different models. A theoretical analysis is held that produced new and improved equations about Cockcroft-Walton's voltage gain as well as new

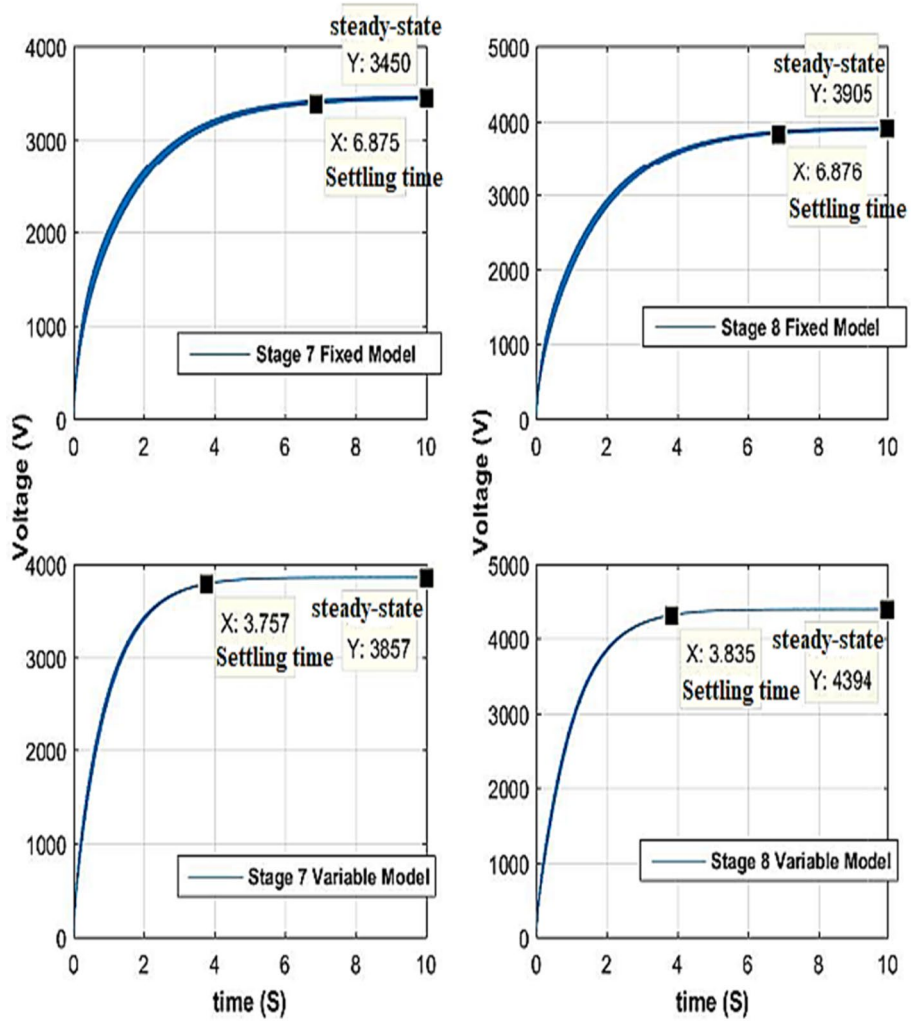

Fig. 11 Settling time, transient and steady state value of output voltage of stage one and two of both models

formulas are introduced that give the Optimal number of stages that provide the proper voltage gain. The theoretical analysis and the simulation in MATLAB/ SIMULINK R2015b reveals that the Variable model is an Optimal design of the Cockcroft-Walton voltage multiplier due to its higher performance, higher output voltage per stage and a less voltage ripple.

When higher magnitude of output high voltage DC supply is required without changing the input transformer voltage level, the Cockcroft-Walton Voltage multiplier circuit is used. It is used only in special applications where the input voltage stability is not critical. This kind of high voltage DC power supply test set is of simple control; low cost, portable due to its light weight robust and high reliability. Different high voltage DC output magnitudes are taken from different stages without changing the input voltage.

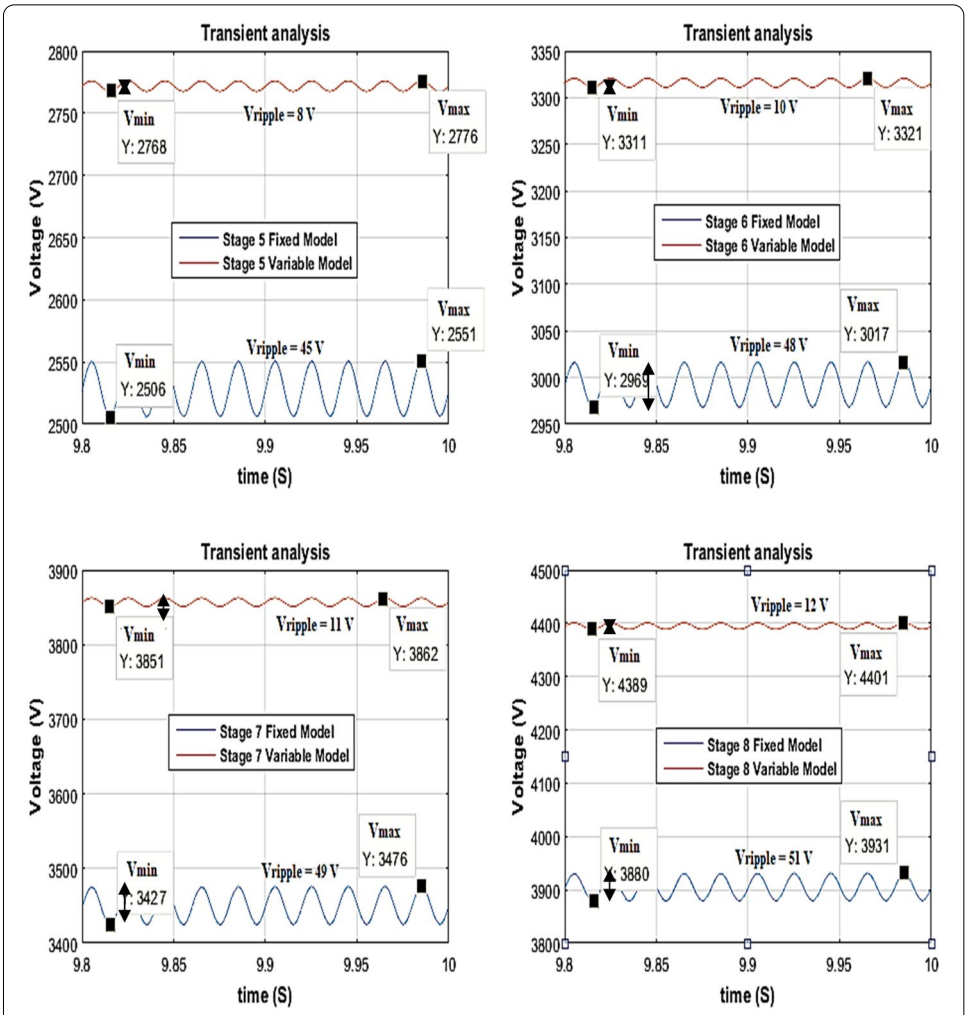

Fig. 12 Voltage ripple comparison

Our work can be enhanced to generate an HVDC up to the range of 25–50 kV by increasing the number of stages thus it will be very useful for field testing of HV cables of different voltage grade, as a DC source for impulse charging unit of impulse generators.

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Author contributions
All authors have read and approved the manuscript. Pierre Kenfack made all the simulation work with the help of Edung Fabrice Nkale. Abraham Dandoussou helped Pierre Kenfack with the basics of the experiment and how to use some key functions of MATALB®. Edung Fabrice Nkale helps the team with proofreading of the manuscript to make it academically appropriate. All authors read and approved the final manuscript.

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Data Availability
The datasets analyzed during the current study are available from the corresponding author or reasonable request.

Declarations

Competing interests
I confirm that I have read SpringerOpen's guidance on competing interests and have included a statement indicating that none of the authors have any competing interests in the manuscript. The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this manuscript. The authors declare no conflicts of interest regarding the publication of this manuscript.

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