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A low-power 8-bit 1-MS/s single-ended SAR ADC in 130-nm CMOS for medical devices

Dina M. Ellaithy[1*]

*Correspondence:
dina_elessy@eri.sci.eg

[1] Microelectronics Department, Electronics Research Institute (ERI), Ministry of Scientific Research, Cairo, Egypt

Abstract

Rapid advancements in micro-machining and microelectronics over the last few years have accelerated the growth of implanted medical devices that greatly improve a person's life. These devices first gather the signals from different nodes in/on the body, and then, they condition, multiplex, and digitize the signals. Thus, an analog-to-digital converter (ADC), which must continuously convert a variety of analog electrophysiological signals to digital codes, is one of the most crucial and power-hungry components. For implantable medical devices, the successive approximation register (SAR) ADC is a good choice. In this paper, a low-power single-ended SAR ADC architecture is proposed to offer good compromises between power efficiency, conversion accuracy, and design complexity. The proposed architecture supports 8-bit resolution at a sampling rate of 1 MS/s. Using a 130-nm CMOS process with 1.2 V supply voltage, an effective number of bits (ENOB) of 7.3 dB is achieved while 28.5 µW power is consumed. The ADC core only occupies an active area of about 197 µm × 377 µm.

Keywords: Bootstrap switch, Capacitive DAC (CDAC), Dynamic comparator, Low power, SAR ADC

Introduction

Electrical systems and devices that can be implanted have be subjected to considerable conversion over the last 60 years, evolving from a useful biomedical tool to wirelessly monitor and measure physiographic reactions in the human body [1, 2]. The development of electronic technologies that can interact with bio-tissues and organs at the micro and nanoscales, as well as a growing understanding of many aspects of the human nervous system, has been essential for the conception and subsequent development of these devices. A large number of small wireless electronic devices (e.g., sensors, smart gastric/cardiac pacemakers, cochlear implants, and implantable cardioverters defibrillators, as well as deep brain, nerve and bone stimulators) have been implanted into patients worldwide [3, 4] due to recent development in electronics especially the smaller size and lower energy demands as shown in Fig. 1. The detected signal can be processed by the signal processing block through an analog-to-digital converter. The converted signal can then be transmitted outside the human body through the signal communication block. All of these mentioned blocks must be powered by energy-harvesting units that capture energy from the human body or the

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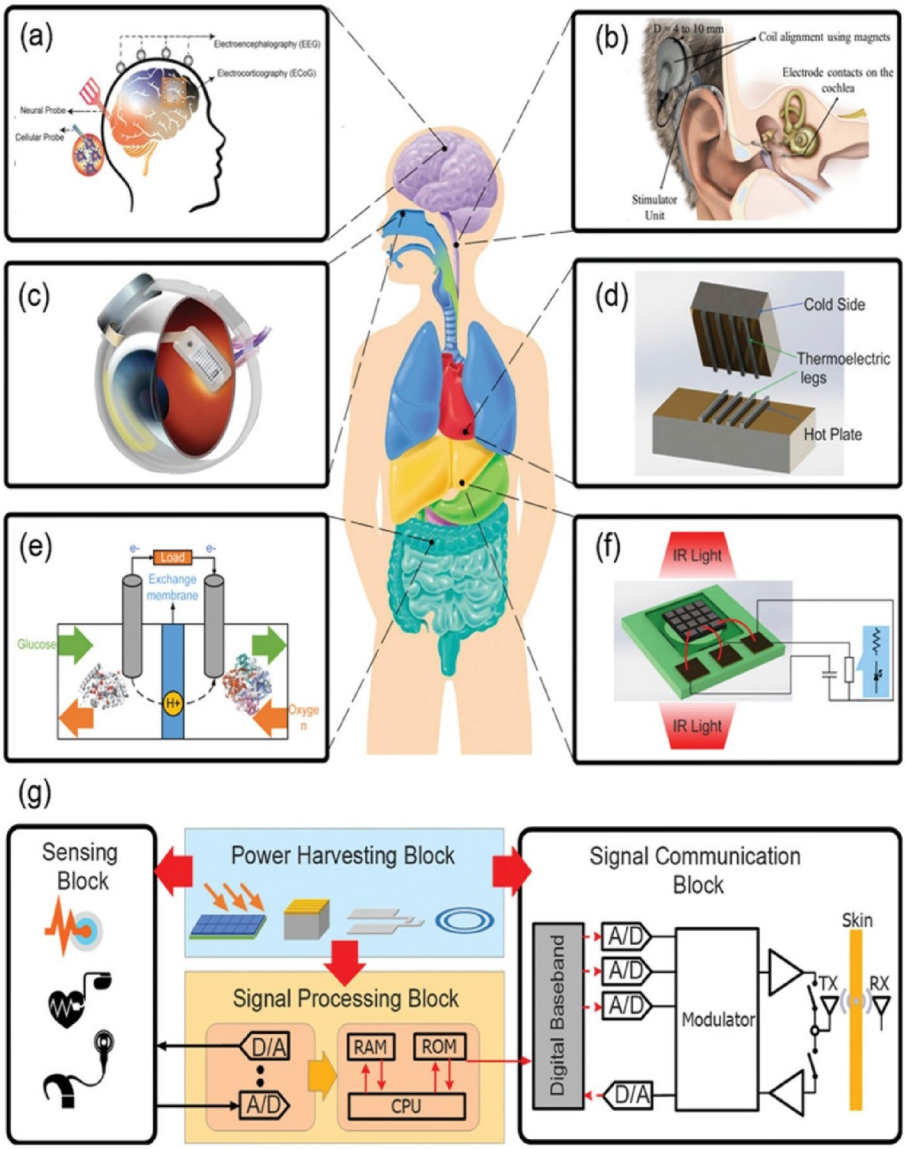

Fig. 1 Different wireless implantable biomedical devices [3]

environment. Additionally, all of these blocks communicate with biomedical sensors or actuators under the skin. The data detection and conversion blocks are capable of detecting physiological data from the human body and converting it into electrical signals. These signals can be processed and stored as readable data using a signal processing module. All this data are then transmitted and received through the tissues using the signal transduction block [3].

Implantable electronic technologies have contributed significantly to improving survival rates and quality of life. In addition, implantation can be seen as a means to enhance the abilities and experiences of the healthy beyond a medical condition. The big challenge faced by the implementation of these battery-powered medical devices is how much these devices are power efficient. Analog-to-digital converters (ADCs)

are one of the most necessary components because they translate the analog collected signals from sensors into to be digitally processed [5]. Due to the critical operations of these devices, the employing ADC must be efficient in terms of power consumption.

Successive approximation register (SAR) ADCs are used in medical applications since they are low-power ADCs with moderate resolution and low sampling frequency. SAR ADCs do not consume a lot of power due to their simple architecture [6–9]. Those specifications are appropriate for medical applications.

The rest of this paper is constructed as follows: In section "SAR ADC architecture review", we demonstrate the conventional SAR ADC operation with the details of each block implementation. The proposed circuit implementation of the low-power SAR ADC structure is described in section "Circuit implementation of the proposed SAR ADC". The simulation results of the proposed ADC are presented in section "Simulation results and comparisons". Finally, this paper is concluded in section "Conclusions".

SAR ADC architecture review

Successive approximation register (SAR) analog-to-digital converters (ADCs) are commonly the design of choice for good resolution with low-power applications. These ADCs are perfected for a wide range of applications including portable/battery-powered devices due to their low-power consumption [10–21].

A conventional SAR ADC consists of a sample-hold circuit (S/H), a dynamic voltage comparator, SAR logic control, and a digital-to-analog converter (DAC), as shown in Fig. 2. The sample-hold circuit samples and maintains the analog input voltage V_{in}. The output voltage from the sample-hold circuit $V_{S/H}$ is compared to the output voltage produced by the DAC, V_{DAC}, by the comparator. The SAR ADC makes N comparisons before producing a digital value corresponding to the outcome of the N-bit binary comparison. A binary search technique is used by the successive approximation ADC to convert the input analog waveform into a discrete digital representation before settling on a digital output representation for the current input.

The SAR ADC functions in accordance with the following binary search method as shown in Fig. 3. An example of a 4-bit conversion is presented. The Y-axis represents the

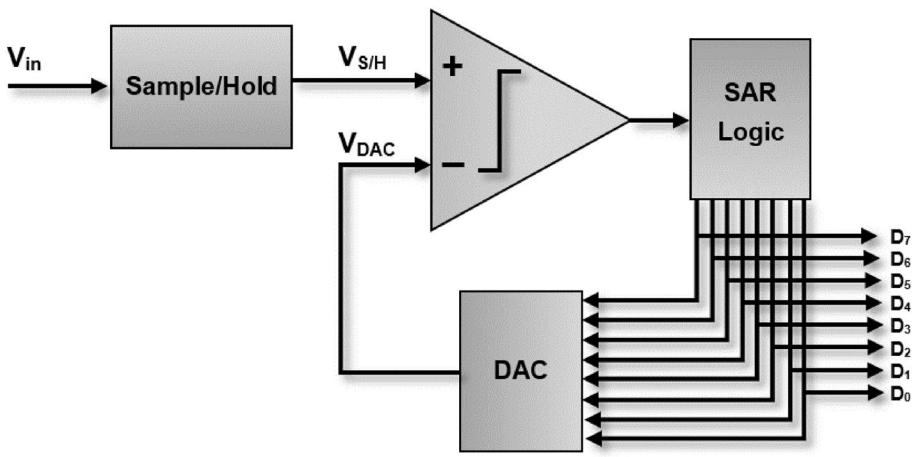

Fig. 2 Single-ended SAR ADC architecture

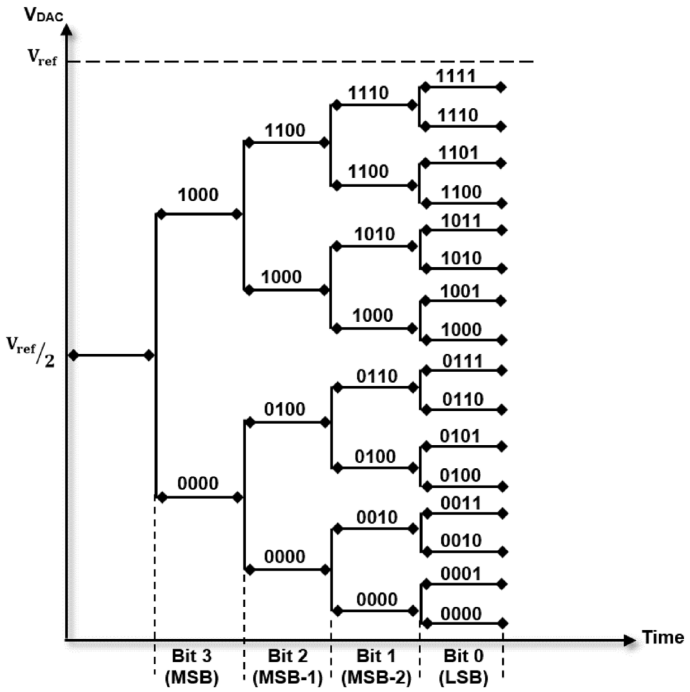

Fig. 3 Four bit conversion SAR ADC

digital output code while the X-axis represents the clock cycles required to complete the conversion.

The SAR's contents are initialized at the beginning of a conversion so that the most significant bit (MSB) is set to a digital 1 and every other bit is set to a digital 0. This code is supplied into the DAC, which provides the comparator circuit with the analog representation of this digital code to compare with the sampled input voltage. Note that this form of code which has only the MSB is set to logic one while the other bits are set to logic zero corresponding to maximum analog voltage over two ($V_{\text{ref}}/2$). The comparator forces the SAR to reset this bit if the analog output voltage from the DAC V_{DAC} is greater than the sampled voltage $V_{\text{S/H}}$; otherwise, the bit is left at 1. This binary search method is then repeated until every bit in the SAR has been tested, after which the next most significant bit is set to 1 and the identical test is performed as shown in Fig. 3. The SAR eventually outputs the code at the conclusion of the conversion, which is a digital approximation of the sampled input voltage. The functions and implementations of each block of SAR ADC are presented in detail in the next subsections.

SAR sample and hold circuit

ADC sample and hold circuits (S/H) hold values between samples of the analog input signal while sampling the analog input signal and remain relevant between clock cycles. The two modes of operation for the S/H circuit are sample mode and hold mode. This often occurs at regular intervals that are determined by a periodic clock that separates circuit operation into two phases. The circuit's output can either track the input during the sample mode or be reset to a predetermined value.

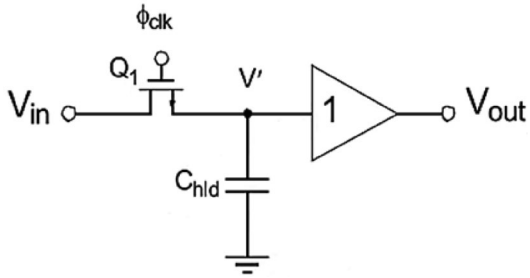

Fig. 4 MOS-based sample and hold circuit

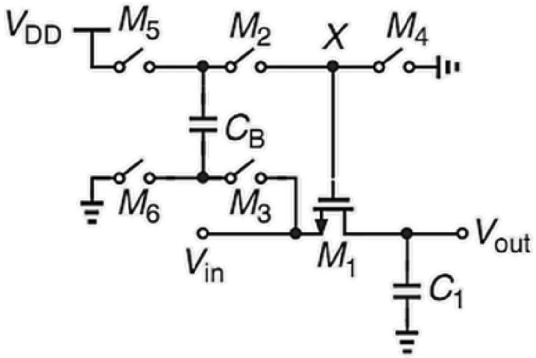

Fig. 5 Implementation of bootstrapped switch [23]

The MOS transistor is the simple choice to create a switch [22]. Figure 4 depicts the fundamental S/H circuit. A capacitor is used from the integrated circuit technology in the hold phase. The current sample and hold circuits have limitations, such as the inability to hold multilevel logic, reliance on the clock signal, and lack of a reference voltage. Metal-oxide semiconductor (MOS) sampling switches show two sources of distortion: their channel charge and on-resistance are dependent on their gate-source voltage (V_{GS}), and therefore on the level of the analog input. If V_{GS} is kept constant during the sampling phase, for example, by connecting a battery between the gate and source terminals, these effects can be reduced [23]. Because the voltages of the two vary in tandem, we refer to the gate as being "bootstrapped" to the source. The switch on-resistance is decreased by using the bootstrapped MOS switch depicted in Fig. 5.

As shown in Fig. 5, M2 and M3 are activated in the sample mode. While in the hold mode, M4–M6 are turned on, grounding M1's gate and connecting the C_B to V_{DD}, to start to charge.

Dynamic comparator

One of the important components of SAR ADC converters is the comparator. The comparator significantly affects the performance of the entire ADC. It creates a digital output of "0" or "1" that will be used in the SAR logic by comparing the analog sampled input to the analog output of the DAC. The block diagram of a traditional single-supply voltage comparator is shown in Fig. 6. If the input voltage to the non-inverting terminal $V_{in,1}$ is greater than the input voltage to the inverting terminal $V_{in,2}$, the produced output

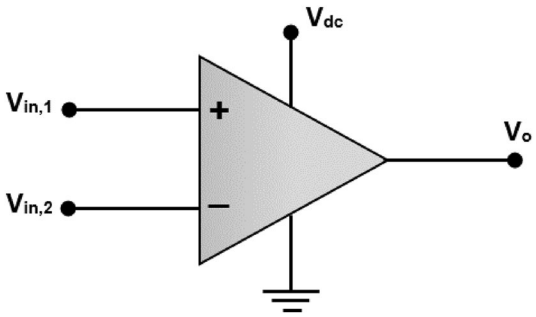

Fig. 6 Traditional single-supply voltage comparator

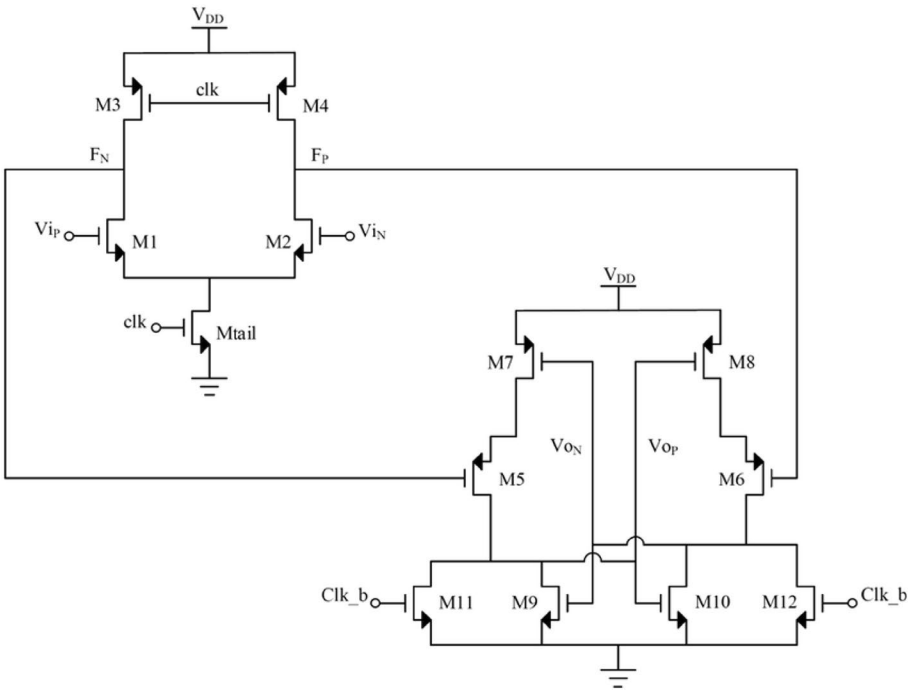

Fig. 7 Dynamic latch comparator [21]

V_o goes to V_{dc}. On the other hand, if the input voltage to the non-inverting terminal $V_{in,1}$ is less than the input voltage to the inverting terminal $V_{in,2}$, the produced output voltage V_o goes to the ground. As it needs to resolve voltages with slight variances, accuracy, and speed are two crucial criteria. The comparator is the main component of the SAR ADC. It must be more accurate than the least significant bit. Also, the comparator power consumption needs to be kept at an extremely low level. As a result, the static energy of the traditional amplifier-based comparator should be decreased. A two-stage dynamic comparator has been used to vanish the static energy; it is employed to compare the analog voltage on the DACs with the sampled input voltage [21, 24]. A dynamic preamplifier serves as the first stage, while a latch serves as the second as shown in Fig. 7.

The inputs are preamplified before being provided as input to the dynamic comparator. A latch forms as a result of the cross-coupled inverters connected across one

another. The latch structure of the dynamic comparator isolates the inputs from the output once the differential voltage is unavailable in the circuit, which is necessary because the applied inputs can change. There are two operational phases: reset and regeneration. During the reset phase, the output nodes are either discharged to the ground or charged to the supply voltage, depending on the architecture of the comparator. In the regeneration phase, the positive feedback creates a digital value at the comparator output, and in the reset phase, the comparator tracks the input. One advantage of dynamic latching comparators is their power efficiency, as they only draw power during regeneration and do not require any during the reset phase. Dynamic latched construction is the comparison implement that consumes the least amount of power. However, because of the significant input referred offset it introduces, it is not recommended for high-resolution ADCs. One can widen the differential pair's input transistor width to mitigate this impact. Preamplifier employment additionally helps in lowering the offset voltage. On the other hand, offset reduction is only achievable at the cost of higher power consumption.

SAR capacitive DAC array (CDAC) architecture

The CDAC is a capacitive array as shown in Fig. 8, where the sampled signal is stored at the beginning of the conversion and the charge is redistributed among all the capacitors to approximate the sampled voltage. The capacitor array is a binary-weighted array. The chosen switching schemes affect the power consumption of the converter. The DAC has different topologies and switching algorithms [21]. A lot of researchers made efforts to reduce the power consumption of SAR ADCs by employing different configurations of the capacitor array in CDAC [12, 13]. By using the capacitor array technique, CDACs are the preferred architecture for biomedical detection applications due to their low complexity, optimized power, and better matching.

The comparator's reference voltage is set to ground in order to find the sign of the voltage difference between its inputs. The comparator output is low and the MSB is set to 0, if $V_{\text{in}} < V_{\text{ref}}/2$, which implies that $V_{\text{a}} > 0$. Conversely, if $V_{\text{in}} > V_{\text{ref}}/2$, then $V_{\text{a}} < 0$; as a result, the comparator output is high and the MSB is set to 1. The

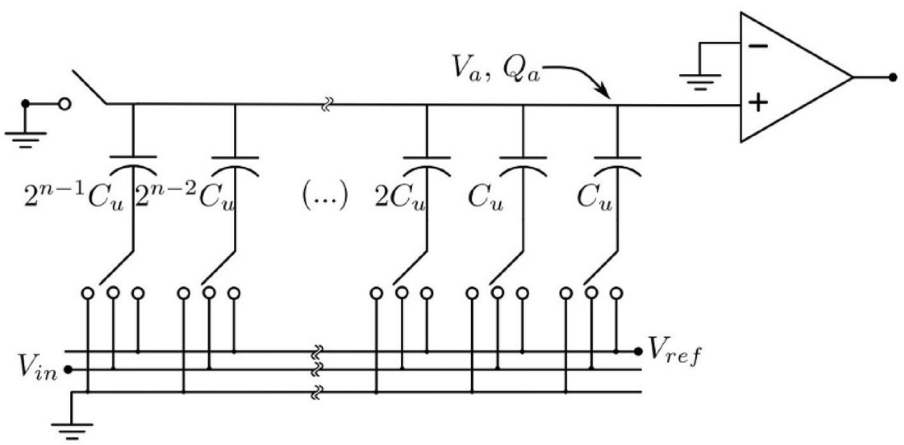

Fig. 8 Single-ended CDAC

capacitor toggles to ground if the MSB is set to 0, but it stays attached to V_{ref} else. The same action is repeated in the following cycle when the capacitor of the MSB-1 bit is connected to V_{ref}, increasing V_a by $V_{ref}/4$.

SAR control logic

Successive approximation register utilizes SAR control logic to implement the binary search technique. The design of the SAR logic can be approached in essentially two fundamentally different ways including sequence and non-redundant SAR logic. The sequence SAR logic consists of a code register and a ring counter as shown in Fig. 9. Based on the output of the comparator, SAR control logic decides the value of bits in a sequential manner. SAR is operating in reset mode, and all outputs are 0 during the initial clock cycle. Data are translated, and each bit is decided consecutively during the course of the following 10 clock cycles [25]. The results of the entire conversion are stored during the final cycle. While the non-redundant SAR uses the fewest possible flipflops. These FFs estimate the converted result and store it. This construction is based on the state of each bit with the state of the bits before. Due to the simplicity of the design process of the sequence SAR logic architecture described in Fig. 9, it is frequently utilized in SAR ADCs [10].

Circuit implementation of the proposed SAR ADC

For better sampling and higher accuracy, a bootstrap sampling switch S/H has been designed as shown in Fig. 10 with different capacitance values to obtain good performance. Due to the nonlinearity of the simple MOS transistor switch, the bootstrap mechanism is employed to decrease the distortion. The on-resistance of the sampling switch is expressed as:

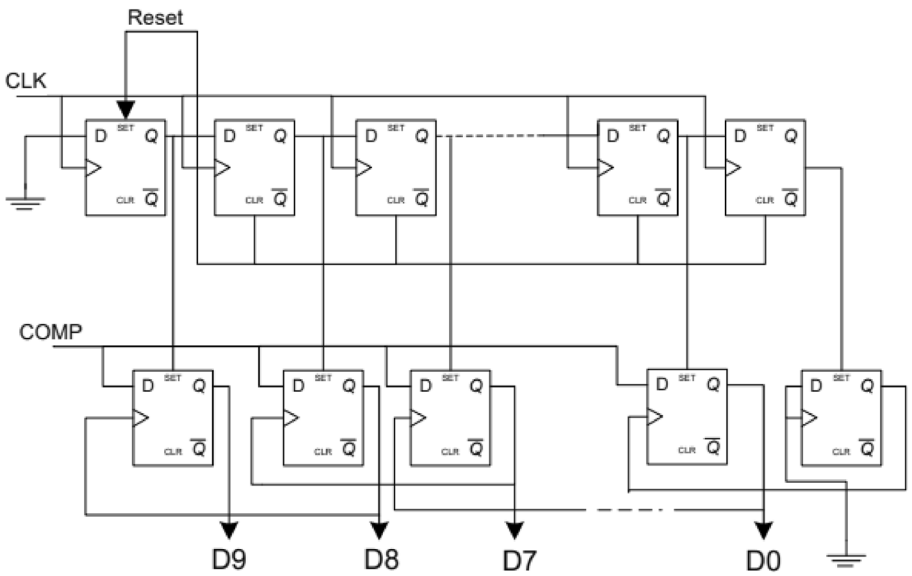

Fig. 9 SAR logic block diagram [25]

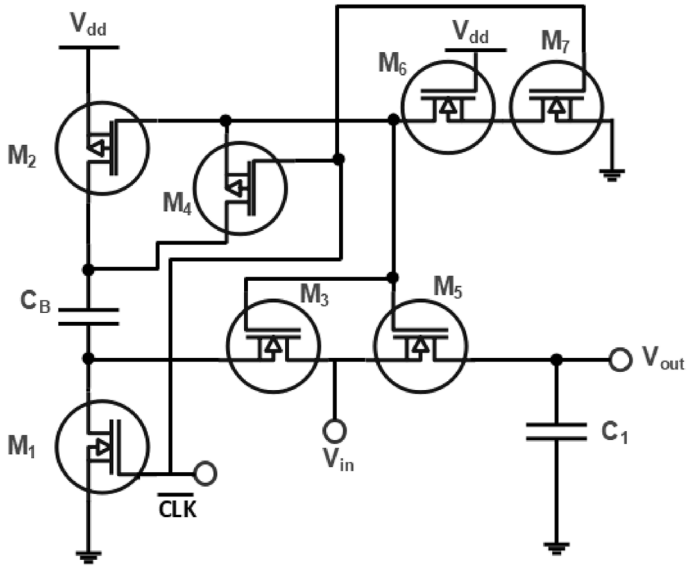

Fig. 10 Proposed bootstrap switch circuit diagram

$$R_{\text{on}} = \frac{1}{\mu_{\text{n}} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{TH}})} \tag{1}$$

The on-resistance depends mainly on the variations of the gate-source voltage. In order to maintain a stationary on-resistance value, the capacitor CB is inserted to obtain the effect of a battery between the gate and the source of the switch transistor M5. During the sample mode, MOS transistors M3 and M4 are on. While the rest MOS transistors are on during the hold mode connect the gate of M1 to the ground and supports CB to charge to Vdd.

Furthermore, in order to decrease the power consumption and obtain low offset voltage, the comparator is implemented by using two stages as shown in Fig. 11. The PMOS preamplifier in the first stage cascaded with a PMOS latch in the second stage is employed. The preamplifier's main role is to amplify the input analog signals to reduce the offset voltage, and the latch's role is to compare the amplified signals from the preamplifier. Power consumption, offset voltage, and delay are the three main performance parameters for the comparator. The comparator determines which of the two input signals has a bigger value by comparing them and producing an output.

When CLK is kept low in the reset phase, the preamplifier starts running, and the output points out1 and out2 are turned to high. The output of the second stage Vo + and Vo- is turned to low. On the other hand, when CLK is set high in the generation phase, the output terminals out1 and out2 of the preamplifier are switched to discharge according to the input voltages. Furthermore, the decision generated at the output terminals of the latch stage depends on the out1 and out2 that rely on the two input voltages Vin + and Vin − .

In the SAR logic architecture, the straightforward structure by [26] is employed. We use D-flipflops that are implemented by simple two-input NAND and three-input NAND as shown in Fig. 12.

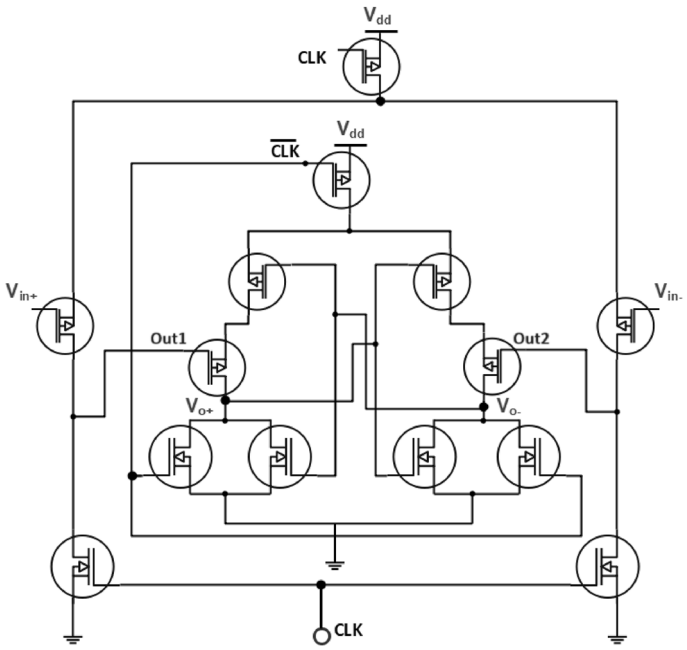

Fig. 11 Proposed dynamic comparator circuit diagram

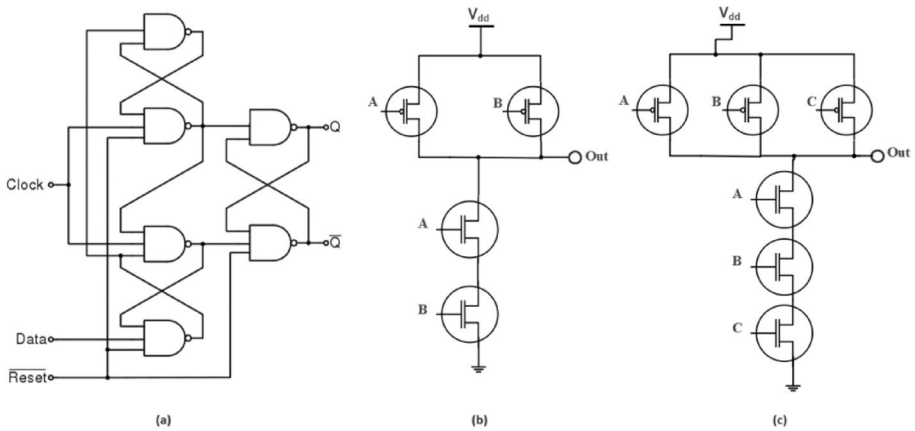

Fig. 12 D-flipflop: **a** Logic diagram of D-FLIPFLOP, **b** implementation of two-input NAND, and **c** implementation of three-input NAND

The traditional capacitive digital-to-analog converter (CDAC) consists of nine weighted capacitors and eight switches as shown in Fig. 13. The first two capacitors' value is the same as the unit capacitors' values being determined according to the process. Thereafter, the capacitor value is doubled in each branch going from left to right. Instead of using a single NMOS transistor to implement the switches, the transition gates implemented by NMOS and PMOS transistors are utilized in the proposed design as shown in Fig. 13. This configuration has better transconductance parameters in comparison with the single NMOS configuration. Additionally, the complementary PMOS and NMOS switches are employed to reduce clock feedthrough problems and charge injection.

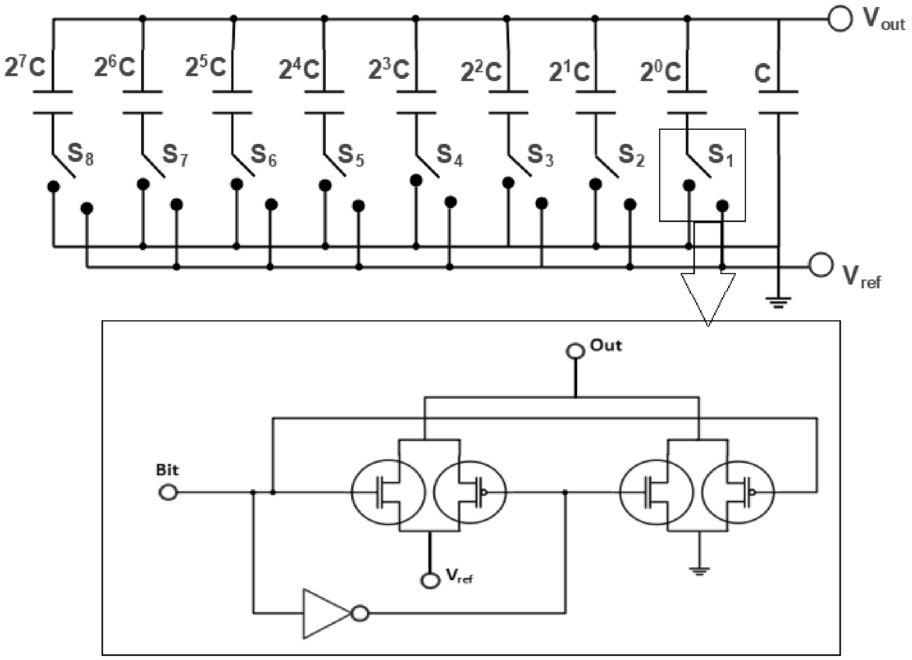

Fig. 13 Proposed binary-weighted capacitor array DAC circuit diagram

The value of the V_{dac} (output of the CDAC) is given by the following equation:

$$V_{out} = \frac{V_{ref}}{2}\left(\frac{b_7}{2^0} + \frac{b_6}{2^1} + \frac{b_5}{2^2} + \frac{b_4}{2^3} + \frac{b_3}{2^4} + \frac{b_2}{2^5} + \frac{b_1}{2^6} + \frac{b_0}{2^7}\right) \quad (2)$$

Simulation results and comparisons

With a 0.13-µm CMOS process, 1.2 V supply voltage, Cadence virtuoso tools, the proposed 8-bit SAR ADC has been implemented. The sampling frequency is equal to 1 MS/s. Figure 14 demonstrates the circuit schematic of the proposed S/H switch. The layout of the proposed S/H switch is shown in Fig. 15, with an active area of $35 \times 90.90 = 3181.5\ \mu m^2$.

Furthermore, Fig. 16 shows the circuit schematic of the proposed dynamic comparator. The dimensions of the input preamplifier transistors of the comparator are designed large enough to get low offset voltage and sufficient preamplification gain for the speed and latch offset reduction. The transient analysis of the dynamic comparator is demonstrated in Fig. 17. As shown, if $V_{in+} > V_{in-}$, out_+ (The output node of the latch) is gradually charged to V_{dd}. If $V_{in+} < V_{in-}$, out_+ (The output node of the latch) reaches ground. Figure 18 presents the layout of the proposed dynamic latch comparator. The performance of the proposed dynamic comparator is listed in Table 1.

The proposed SAR logic register is implemented by employing eight D-flipflops for the counter and eight D-flipflops for the logic register. The SAR logic register schematic is demonstrated in Fig. 19. The transient analysis shows how the SAR logic works as shown in Fig. 20. The SAR logic feeds the comparison result to the D input of the D-flipflop. If the generated voltage is higher than the input signal, the D-flipflop is set to "1",

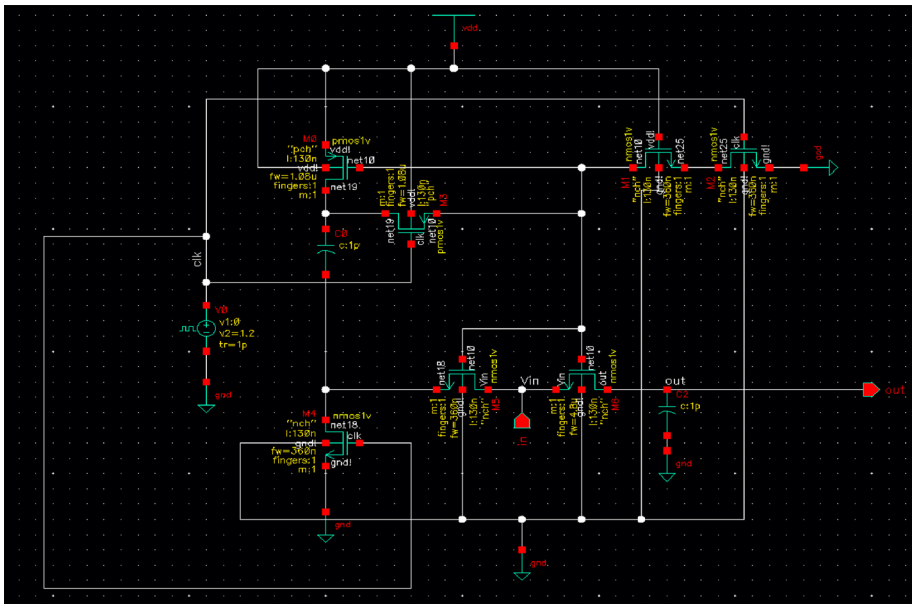

Fig. 14 Proposed bootstrap sampling switch S/H in Cadence Virtuoso

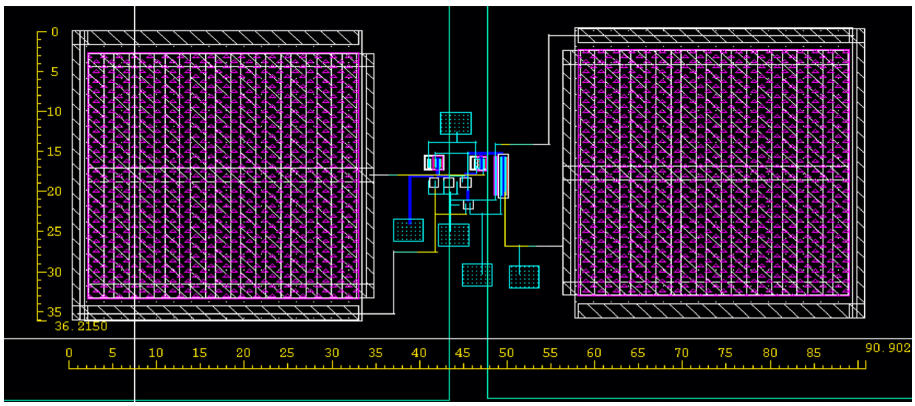

Fig. 15 Bootstrap switch S/H layout

indicating that the current bit is “1". Otherwise, it is reset to “0". This goes on till the last flipflop in the SAR Logic. It is shown that it has an active area of $86.8193 \times 353.4870 = 30{,}689.4939$ μm^2 as shown in Fig. 21.

The circuit schematic of the CDAC is shown in Fig. 22. Also, the implementation of the proposed switch is presented in Fig. 23. Different values of bits were also tested, and a comparison between the theoretical and practical values is demonstrated in Table 2. The proposed CDAC occupies an area of $91.9 \times 257.5140 = 23{,}665.5366$ μm^2. The layout of the proposed switch and CDAC is shown in Figs. 24 and 25.

The transient analysis of the proposed SAR ADC is shown in Fig. 26. As shown in the waveform, the analog signal is sampled and held. Then, the comparator compares the output of the sample and hold (V_{in+}), and the output of the capacitive DAC (V_{in-}). Note that the output of the V_{in-} is set to midscale at first (0.6 V). If the value of V_{in+}

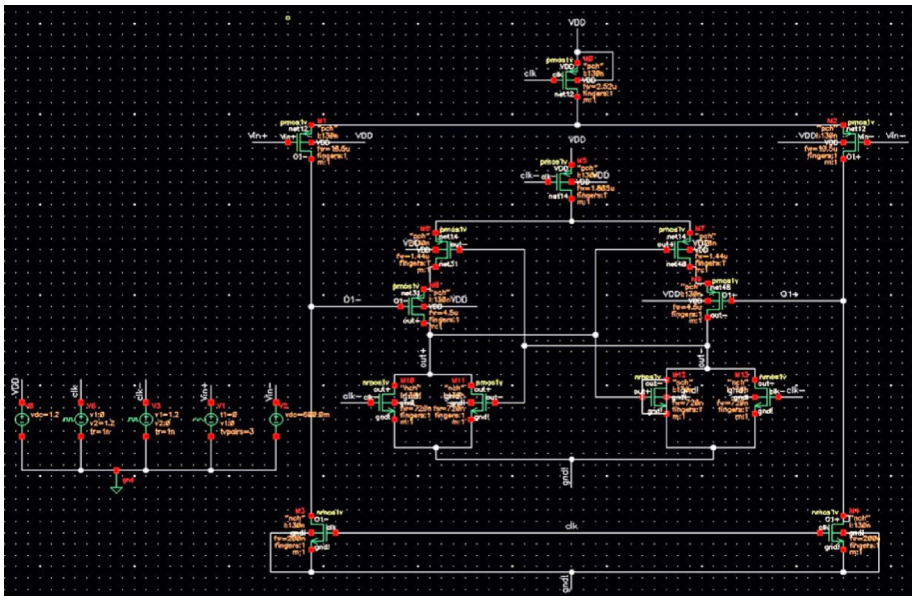

Fig. 16 Proposed dynamic comparator in Cadence Virtuoso

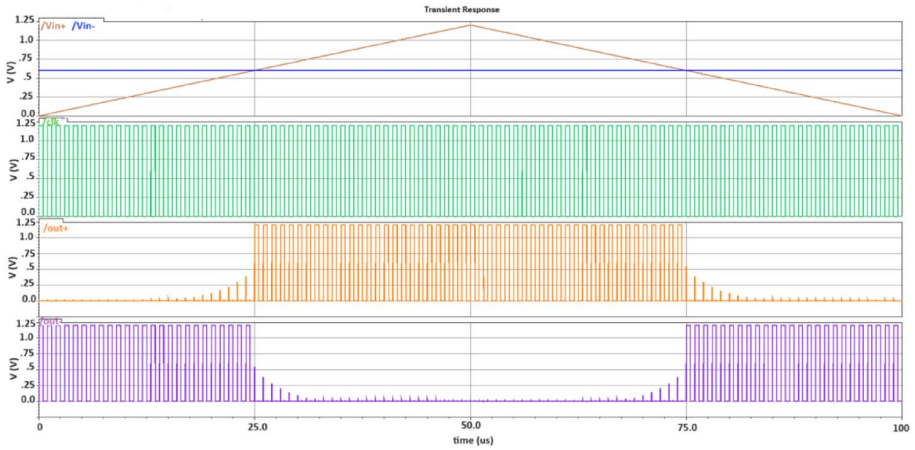

Fig. 17 Clock, input, output waveforms of PMOS preamplifier cascaded with a PMOS latch

is greater than that of $V_{\text{in}-}$, then the output of the comparator becomes high and the MSB of the SAR logic register remains 1; otherwise, if the comparator output is low, the MSB of the SAR logic register becomes 0. This goes on till the last bit. The layout of the proposed ADC is presented in Fig. 27 with an active area of $196.9420 \times 376.7180 = 74{,}191.5964 \quad \mu m^2$. The performance of the proposed SAR ADC and work [14–20] is listed in Table 3. For the comparison to be fair enough, the resolution of most work in Table 3 is 8-bit and the sampling rate is 1 MS/s. A low-power consumption is achieved by the proposed ADC. Furthermore, a less active area is occupied by the proposed structure. This work achieves an effective number of bits (ENOB) of 7.3 dB, consumes 28.5 μW, and occupies 0.0742 mm^2.

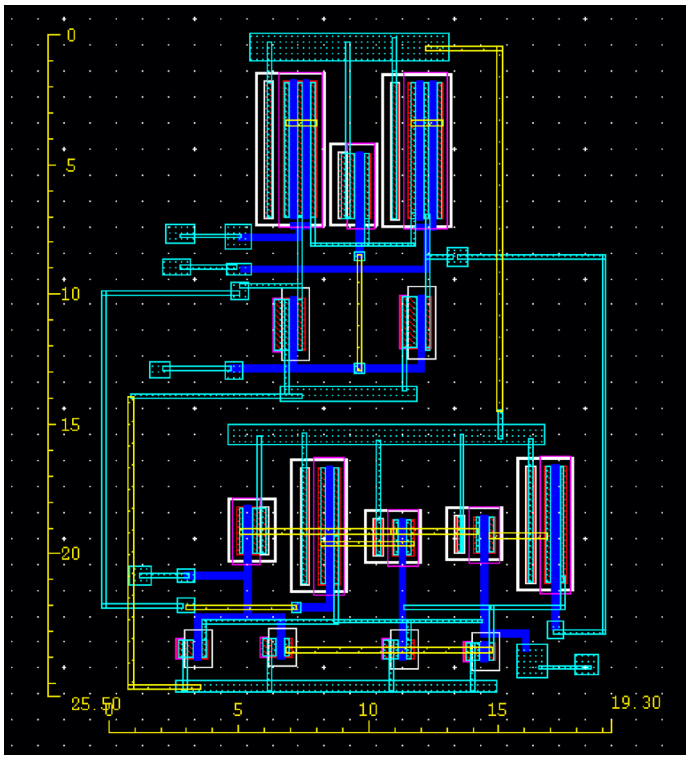

Fig. 18 Dynamic latch comparator layout

Table 1 Performance of the proposed dynamic comparator

Power	132.1 nW
Delay	680 ps
Offset voltage	25.87 μV
Area	$25.5 \times 19.3 = 492.15$ μm^2

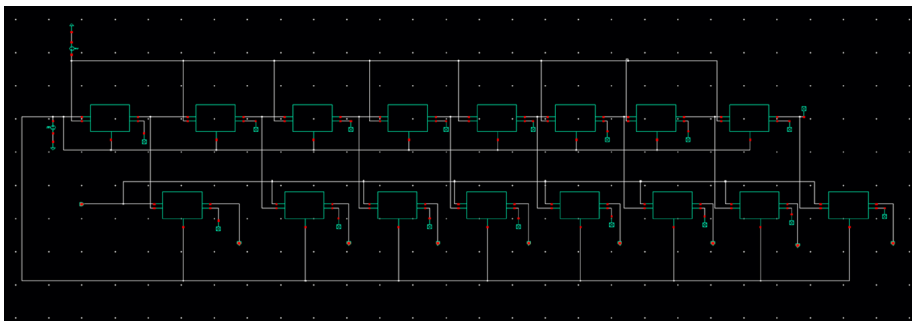

Fig. 19 SAR logic schematic using cadence tool

Conclusions

In this paper, an 8-bit low-power successive approximation register analog-to-digital converter SAR ADC is accomplished. To obtain good performance with low-power

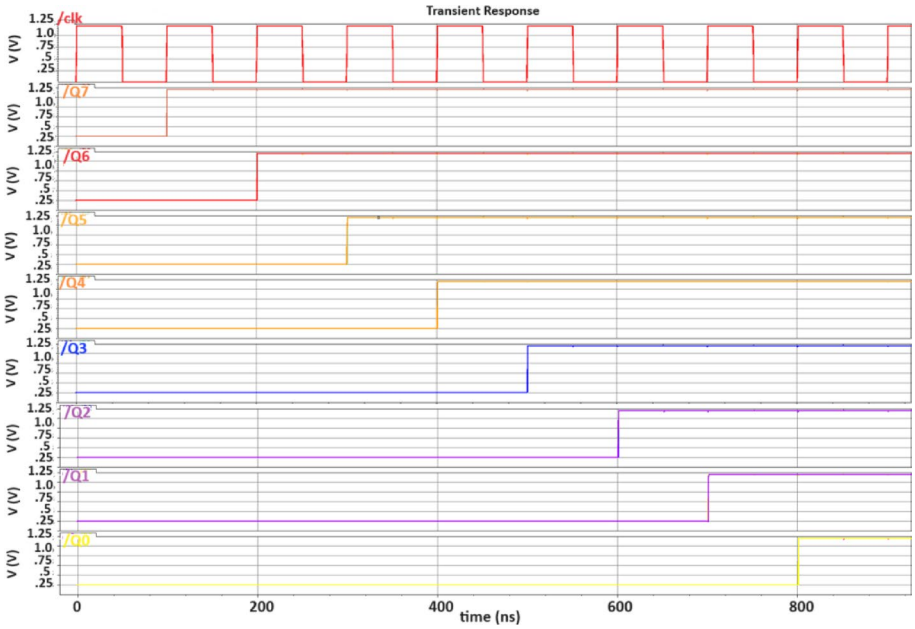

Fig. 20 Waveform of SAR logic register

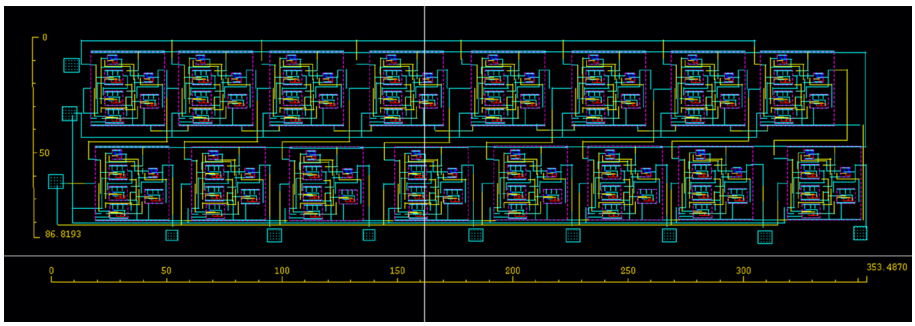

Fig. 21 SAR logic register layout

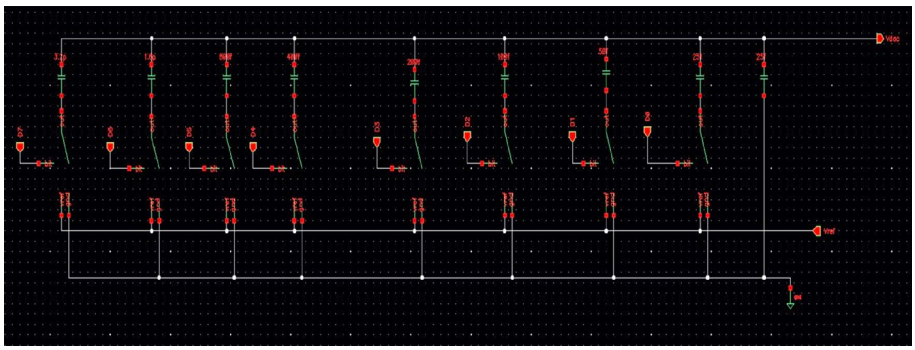

Fig. 22 CDAC schematic using cadence tools

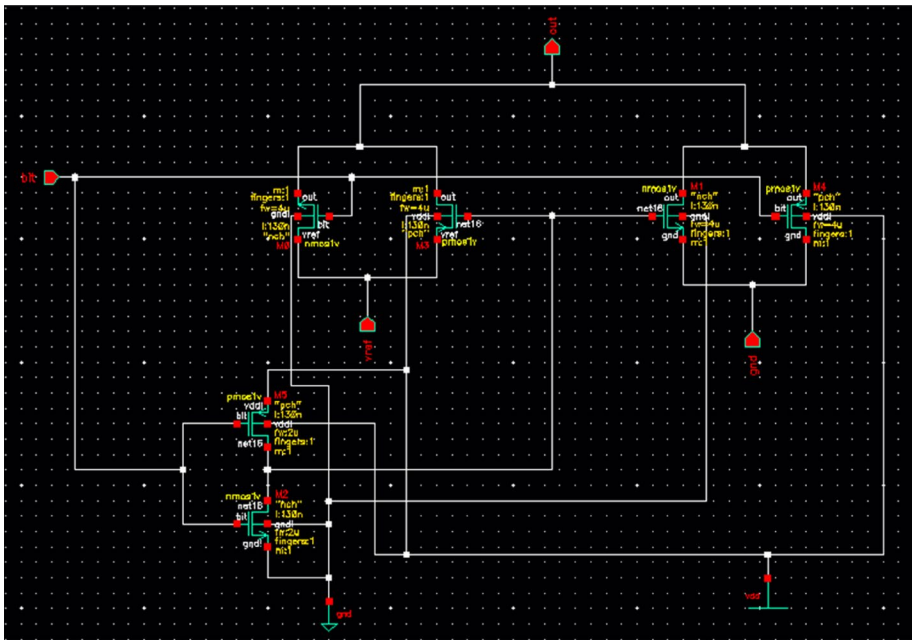

Fig. 23 DAC switch schematic using cadence tool

Table 2 Binary-weighted switched capacitor array DAC simulation results

Digital input	Calculated value (V)	Simulated value (V)
1100 1100	0.95625	0.95625
1111 1111	1.2	1.2
1100 0000	0.9	0.9
1111 0000	1.125	1.125

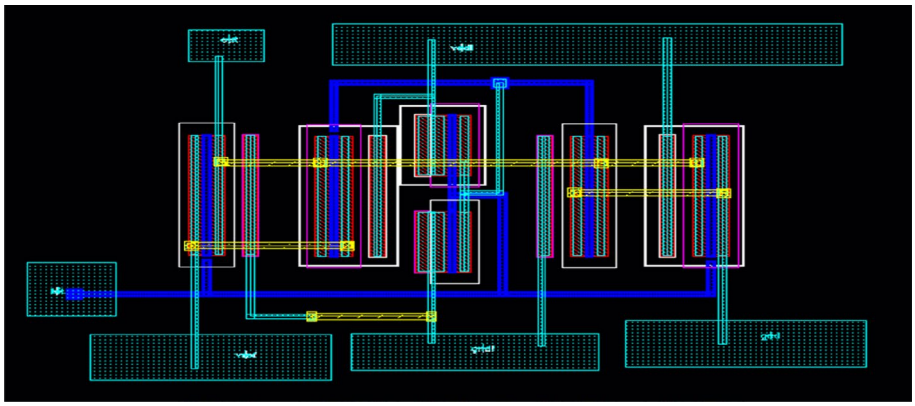

Fig. 24 DAC switch layout

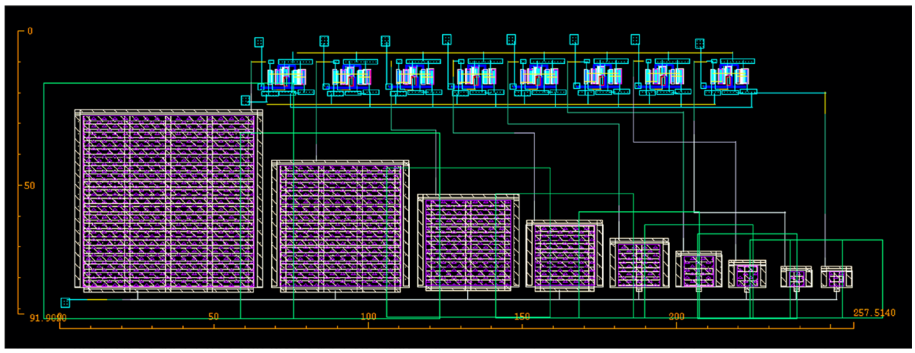

Fig. 25 Capacitive DAC layout

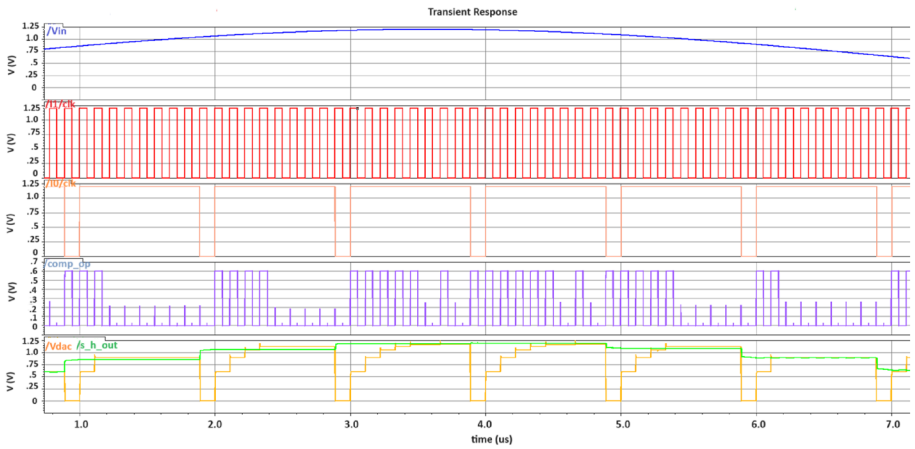

Fig. 26 SAR ADC simulation

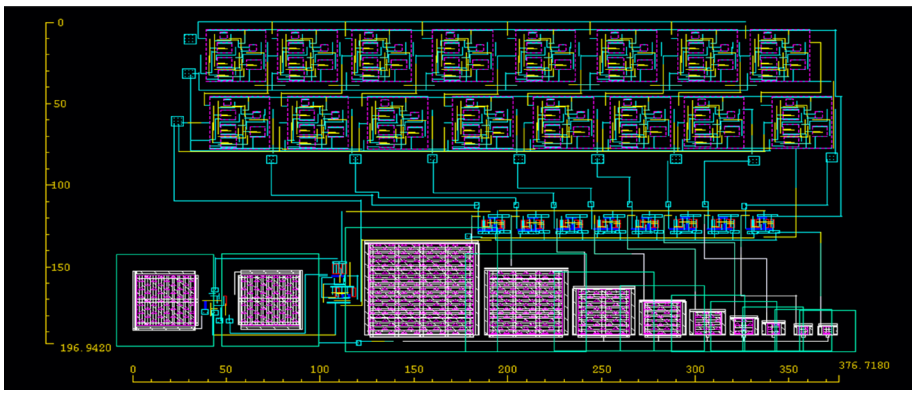

Fig. 27 Proposed SAR ADC layout

Table 3 Summary of the recently published SAR ADC performance parameters

	Process (nm)	Supply (V)	Power (μW)	Area (mm^2)	Fs (S/s)	Resolution (bit)	ENOB (dB)	SNDR (dB)	SFDR (dB)
[14] 2021	500	3.3	21.9	–	10k	8	7.32	–	–
[15] 2018	40	0.9	29.7	0.00986	1M	8	7.29	45.64	63.56
[16] 2019	180	1.5	90.15	–	1M	14	11	67.9	–
[17] 2023	55	1.2	43	0.099	1M	13	11.1	68.5	83.8
[18] 2020	90	1	77.26	–	1M	6	5.91	–	–
[19] 2021	65	1.2	21	–	1M	8	7.9	49.3	61
[20] 2021	180	1.4	44.78	0.3674	1M	12	11.25	69.51	84.95
This Work	130	1.2	28.51	0.0742	1M	8	7.3	45.7	56.5

consumption, a modified bootstrap switch, efficient capacitive array DAC switch, and low-power SAR logic register are proposed. Also, a two-stage dynamic latch comparator is used to enhance the ADC performance. At a sampling frequency of 1 MS/s, 130 nm process, and 1.2 V supply voltage, the proposed SAR ADC achieves SNDR by 45.7 dB and consumes power by 28.5 μW with an active area of 0.0742 mm^2.

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Author contributions
The author has collected data, designed the proposed work, implemented the proposed design, compared the proposed with state of the art, and written, reviewed, and submitted the manuscript.

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Declarations

Competing interests
The authors declare that they have no competing interests.

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