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Voltage-controlled oscillator based analog-to-digital converter in 130-nm CMOS for biomedical applications

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Abstract

Medical implants and portable wireless sensors are the most serious of biomedical applications due to the dependence on limited battery lifetime. Consequently, energy efficiency integrated circuits designs must be put to higher attention. A particular distinguishing contribution of this paper is its focus on the power consumption that affects battery life and the heat dissipated for biomedical applications. This paper demonstrates a power-efficient implementation of analog-to-digital converter (ADC) based on voltage-controlled oscillator (VCO) to convert the collected analog vital signs into digital data for digital signal processing. The current-starved scheme is employed to implement the VCO efficiently with five-stage which leads to high savings in power and area. D-flip flop (D-FF) scheme is proposed to simplify the hardware architecture of the proposed reset counter. The proposed architecture is implemented with 130 nm CMOS technology and it can perform conversion of analog input signal to digital output using a straightforward hardware structure. The proposed VCO-based ADC achieves improvement in energy saving. Simulation results confirm that this work attains a power dissipation of 0.257 mW and active area of 0.007 mm^2, and a very good Walden FOMW of 125 dB. The proposed methodology can implement any number of bits of the ADC by using the appropriate voltage-controlled oscillator with the convenient reset counter.

Keywords: Voltage-controlled oscillator (VCO), Current-starved oscillator, Analog-to-digital converter (ADC), Low power, Reset counter, D-flip flop

Introduction

Currently, the major attention of technological development is on the biomedical applications to improve the quality of healthcare services. Biomedical applications are such as monitoring human vital signs (e.g., heart rate, body motion, blood pulse pressure, blood glucose levels), process physiological data, and transmit the information to allow portable health monitoring [1, 2]. Because most of the biomedical devices are portable and battery-operated devices, energy-efficient implementation is required for all architectures. Since all vital signals are analog, the converting capabilities from analog form to digital form will be necessary for attaining digital advances. The analog-to-digital converter (ADC) is a fundamental component of most of the

biomedical devices. Analog-to-digital converters have a great role in digital processing since they interface the real analog signal to the digital domain [3, 4]. As shown in Fig. 1, sensor nodes are common components in a wireless body area network (WBAN) systems. They serve as the front end for biosensing, collecting data from sensors and transmitting it over the network. Mainly, the sensor node contains a biosensing analog front end, an analog-to-digital converter, a digital signal processing core, a power management unit, and a wireless telemetry section. The task of the ADC is to transform the collecting analog information from sensors into digital data for straightforward processing.

The implementation of analog-to-digital conversion can be performed using a variety of techniques of ADCs. There are several important performance parameters for the ADC design such as sampling rate, effective number of bits (ENOB), signal-to-noise-and-distortion ratio (SNDR), power consumption, area, and figure of merit (FOM). The speed of conversion, power, area, and SNDR required for an ADC in a system are determined by the specific application. The serious constraints on the design of the ADC for biomedical applications are the power consumption. Various architectures of ADC are proposed to trade-off conversion speed, SNDR, and power consumption. In general, each type of ADC performs best in a specific range of sampling rate and resolution [5–8]. Some ADCs, for example, are efficient with high resolutions but only at a low sampling rate, whereas others are very fast but inefficient in high-resolution applications. The voltage-controlled-oscillator-based ADC is a promising architecture to attain high energy efficiency [9–23]. In this scheme, the analog input is converted to a varied-frequency output in the first stage. A voltage-controlled oscillator (VCO) is utilized to perform this operation. Then, a reset counter is employed in the second stage to transform the varied-frequency pulses that generated from the VCO into a digital code. The aim of this paper is to design and implement an energy-efficient VCO-based ADC for biomedical applications. All design architectures are implemented using Cadence Tool in 130 nm CMOS technology.

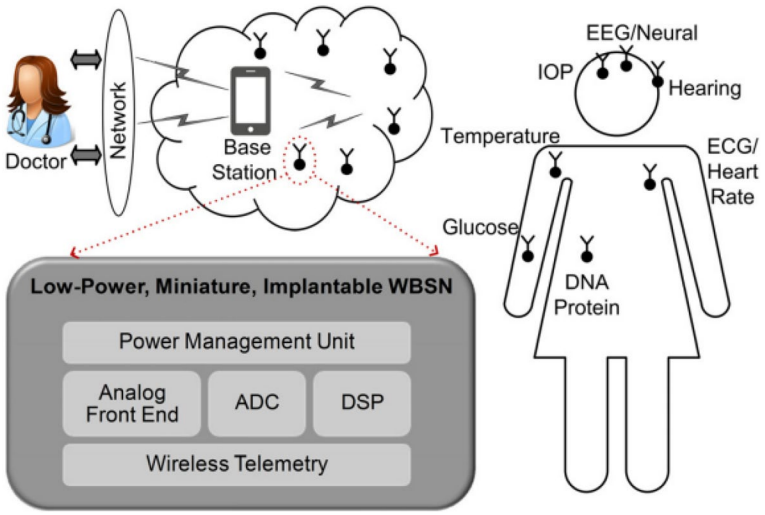


Fig. 1 Sensor node in wireless body area networks [1]

The paper is structured as follows. Sect. "Principle of operation" gives the principle of operation of the VCO, and the reset counter that are employed for the analog-to-digital conversion. Sect. "Proposed design of VCO-based analog-to-digital converter (VCO-ADC)" presents the proposed VCO-based ADC architecture. Hardware implementation and simulation results are discussed in Sect. "Hardware implementation and simulation results." The final section is Sect. "Conclusions," which reports the conclusions.

Principle of operation

Time-based ADCs are considered as indirect type ADC, as it converts the analog signal to digital by an indirect way [9–23]. The analog input is converted into a linear function of time or frequency. Then, this function is converted to an output code which is the digital output.

The VCO-based ADC is considered important type of time-based ADC architectures [13–23]. Figure 2 demonstrates the block diagram of the VCO-based ADC. It uses a VCO as a voltage-to-frequency converter (VFC) and a reset counter as a frequency-to-digital converter (FDC). A voltage-to-frequency converter (VFC) is a voltage-controlled oscillator, which have a frequency that is linearly proportional to the input voltage.

The oscillator's frequency is modulated by the analog varying input signal. A digital counter is then used to count the oscillator's pulses. Given a sampling frequency of fs, the counter is reset after every sampling period T_s seconds, which is $T_s = 1/f_s$. The counter output thus represents the VCO frequency and, consequently, the analog input signal for that sample. A detailed description of the VFC and the FDC is presented in the following subsections.

Voltage-to-frequency converter (VFC)

Due to its high integration capability, wide operating frequency range, and low power consumption, the voltage-controlled oscillator (VCO) plays a crucial role in different application fields [24–30]. A resonant circuit, amplification, and feedback are all used in this electronic device to produce a voltage waveform that repeats at a specific frequency. An applied voltage can change the frequency, or rate of repetition per unit of time. Phase-locked loops, clock recovery circuits, frequency synthesizers, time-based ADCs, and virtually every digital and analog system all rely on VCOs.

High frequency, low power consumption, phase stability, a wide electrical tuning range, frequency linearity on the control voltage, a small area, low cost, and a high gain factor are all requirements for VCO applications. There are trade-offs when

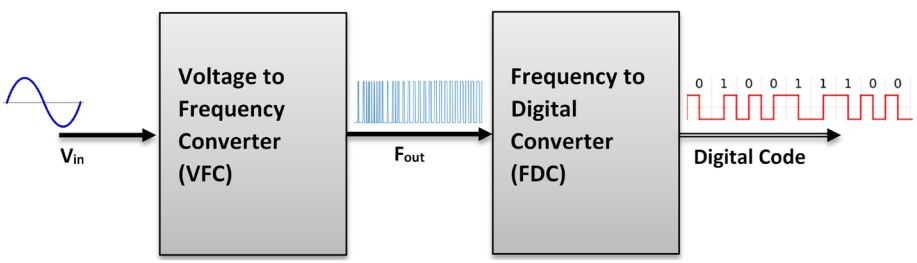


Fig. 2 Block diagram of VCO-based ADC

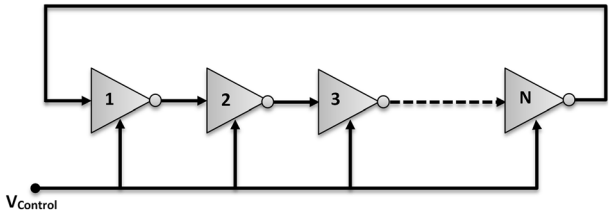


Fig. 3 Conventional N-stage ring oscillator architecture

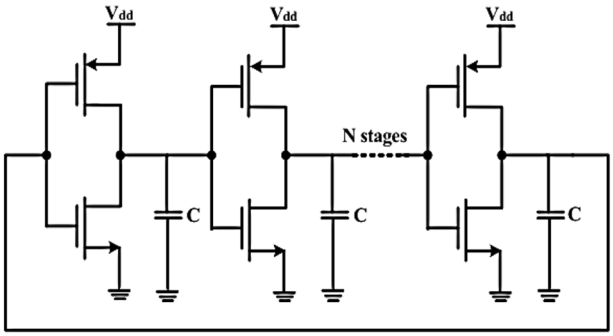


Fig. 4 Schematic of conventional ring oscillator [29]

designing a VCO in terms of area, speed, power, frequency range. The VCO can be implemented by two main types, which are the LC VCO and the ring VCO.

An amplifier is used to construct the LC VCOs using inductors and capacitors [24]. Utilizing inductors and capacitors, voltage-controlled oscillations of a very high frequency are produced. For sinusoidal wave output, this architecture is preferred because it can be integrated with low phase noise and high stability. However, these are traded off with power consumption and area. On the other hand, the ring oscillator [25–30] which is constructed by odd number of inverters connected serially after each other as shown in Fig. 3. A conventional single-ended N-stage ring VCO is presented in Fig. 3. The ring oscillator operates by organizing the charging and discharging of the gate capacitance of the inverters. The periodic time of output signal from the ring oscillator is given by:

$$T = 2 \times N \times t_d \tag{1}$$

where N is the odd number of inverters, and t_d is the delay time of single inverter. Increasing the odd number of the inverters, charging current increases the time to charge and discharge the gate capacitance; consequently, the frequency is decreased. This type of VCO attains wide frequency range of operation without sacrificing power and area. The conventional circuit schematic of the ring VCO is shown in Fig. 4. Each delay stage consists of two MOSFETs, PMOS and NMOS connected to form an inverter. However, frequency of oscillations depends on delay introduced by each inverter stage so delay should be voltage controlled. One way to control the delay is to control the amount of current available to charge or discharge the capacitive load of each stage. This type of circuit is called a current-starved ring VCO [26–30]. Current-starved ring VCO uses variable bias currents to control its oscillation frequency as shown in Fig. 5.

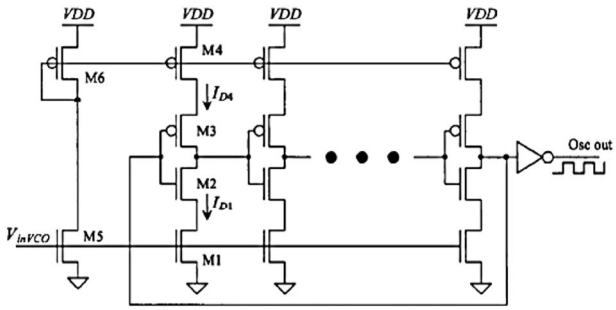


Fig. 5 Schematic of current-starved VCO [23]

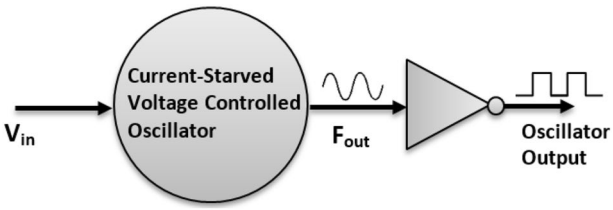


Fig. 6 Block diagram of the proposed voltage-to-frequency converter (VFC)

The transistors M2 and M3 operate as inverters while M4 and M1 operate as current sink and current source, respectively. The current sources limit the current available to inverters. The drain currents of transistors M5 and M6 are same and set by the input control voltage ($V_{\text{in-VCO}}$). The current in transistors M5 and M6 is mirrored from bias stage to each inverting stage [27]. The benefit of this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control voltage. The oscillation frequency is determined by the bias current (I_d), number of stages (N), total capacitance (C_{total}), and control voltage ($V_{\text{in-VCO}}$) as:

$$f_{osc} = \frac{I_d}{N \cdot C_{total} \cdot V_{in-VCO}} \tag{2}$$

The total capacitance is given by:

$$\begin{aligned} C_{total} &= C_{out} + C_{in} = C_{ox}\left(W_pL_p + W_nL_n\right) + \frac{3}{2}C_{ox}\left(W_pL_p + W_nL_n\right) \\ &= \frac{5}{2}C_{ox}\left(W_pL_p + W_nL_n\right) \end{aligned} \tag{3}$$

where C_{out} is the delay cell output capacitance, C_{in} is the delay cell input capacitance, C_{ox} is the oxide capacitance, W_p, W_p are channel widths, and L_p, L_p are channel lengths.

Unlike the basic design of the ring VCO (Fig. 4), there are four MOSFETs in each delay stage in the current-starved ring VCO as shown in Fig. 5.

The block diagram of the proposed voltage-to-frequency converter VFC is demonstrated in Fig. 6. An inverter is used after the current-starved ring VCO to convert the modulated frequency sinusoidal signal into a frequency modulated pulses can be counted by the FDC.

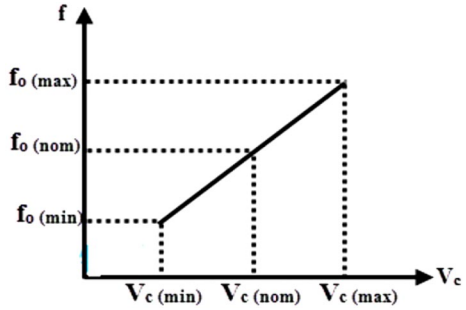


Fig. 7 Voltage-to-frequency tuning curve [23]

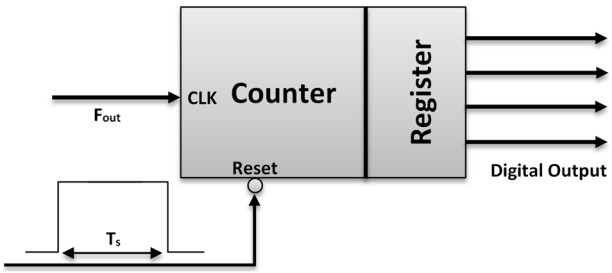


Fig. 8 Block diagram of frequency-to-digital converter FDC

The tuning curve of the VCO is demonstrated in Fig. 7. The ratio of the difference between the maximum frequency and minimum frequency to the maximum frequency is known as the frequency tuning range and is defined as:

$$\text{Tuning range} = \frac{f_{o(max)} - f_{o(min)}}{f_{o(max)}} \tag{4}$$

The minimum frequency is set to be the sampling frequency. For four digital output, the maximum frequency is adjusted to be $2^4 \times$ samplingfrequency. The VCO gain can be defined as the ratio of change in oscillation frequency to the change in the control voltage and is defined as:

$$K_{VCO} = \frac{\Delta f_{osc}}{\Delta V_{in-VCO}} \tag{5}$$

Frequency-to-digital converter (FDC)

The frequency modulated signal is converted to a digital code via FDC [16, 21]. The frequency modulated signal's rising edges are counted and quantized by the FDC during the sampling interval. The architecture of the frequency-to-digital converter FDC is presented in Fig. 8. It consists of a reset counter followed by a register. The VFC output pulses are counted by a digital counter. Assuming that the sampling period is Ts, the number of pulses accumulated in the counter is output to the register every Ts seconds, and then the counter is reset. The code in the register therefore represents the equivalent

of the VCO frequency and therefore of the analog input signal within this sample. Typically the reset counter is implemented by using D-FFs.

The timing diagram in Fig. 9 illustrates how the sampled counting number and the input signal are related to the oscillation frequency of the VCO. When the input voltage is at the minimum level, the VCO output frequency is adjusted to equal the sampling frequency. Consequently, one cycle is fed to the counter that generates one count which is corresponding to the digital output [$D_3D_2D_1D_0$ = "0001"]. While if the input voltage is at the maximum level, the VCO produces output frequency that equals to 16 times the sampling frequency. Thus, the counter outputs 16 counts that represent the maximum voltage input which corresponds to the digital output [$D_3D_2D_1D_0$ = "1111"].

Proposed design of VCO-based analog-to-digital converter (VCO-ADC)

For the required tuning range with higher linearity, a five-stage current-starved VCO scheme is employed to construct the VFC as shown in Fig. 10. The first stage that consists of transistors Mn1 and Mp1 is the biasing circuit which is essential to provide the current to each stage. The input transistor Mn1 accepts the input voltage control sweep from minimum to maximum voltage. Therefore, as long as the input voltage increases, the drain current (I_d) increases and the output frequency increases. The PMOS Mp1 is a diode-connected transistor that mirrors the drain current to the next stages. An inverter is placed after the current-starved VCO to convert the analog output modulated signal to square wave.

A four D-flip flops (D-FFs) are used in order to build a four-bit counter to be able to read the digital output. A counter can have a maximum of 2^n states, where n is the number of flip flops in the counter.

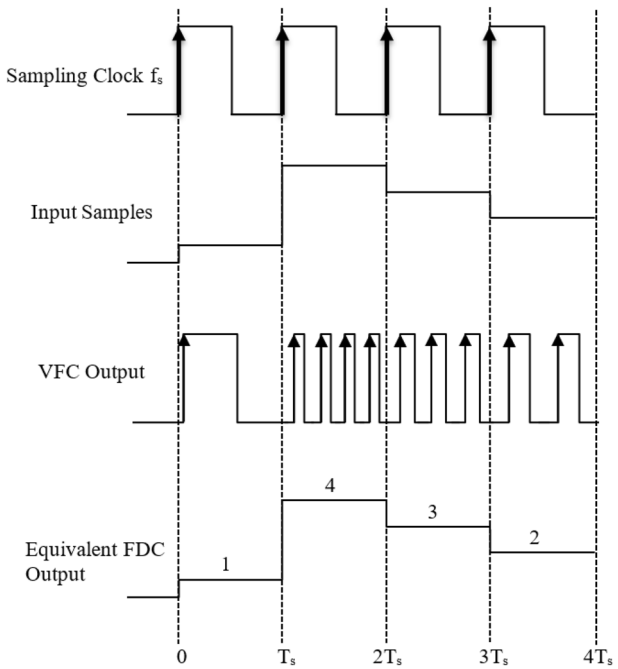


Fig. 9 Timing diagram of the VCO-based analog-to-digital converter (VCO-ADC)

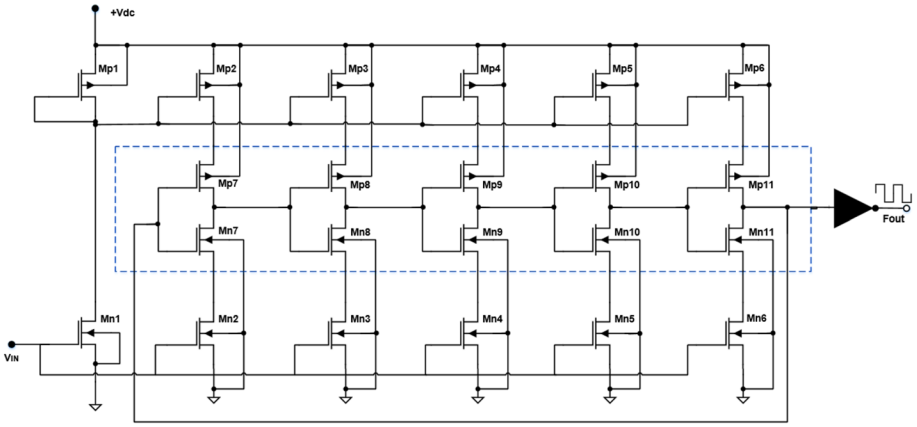


Fig. 10 The proposed five-stage current-starved VCO circuit scheme

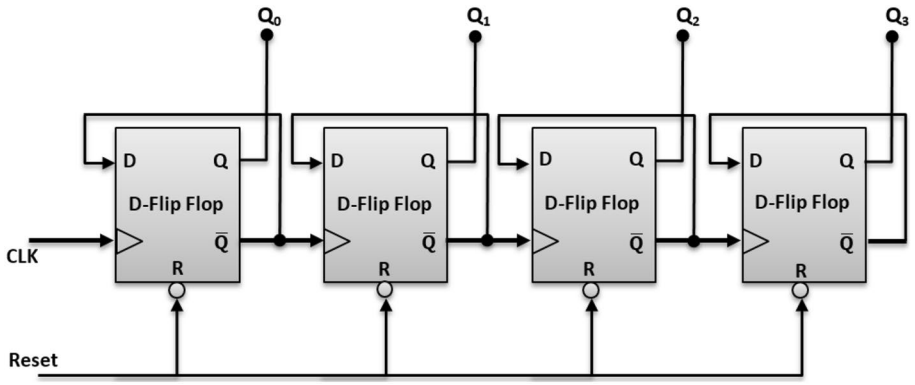
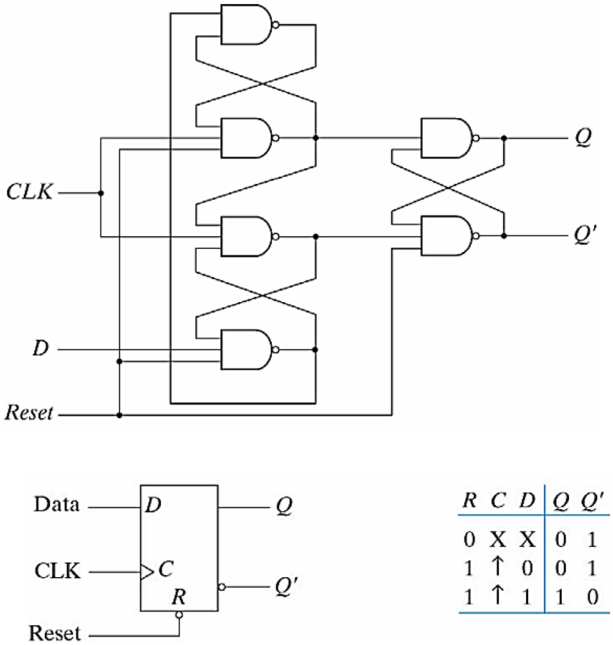


Fig. 11 Proposed frequency-digital-converter (FDC) implementation by using four D-FFs

Figure 11 shows the FDC implementation by using four D-FFs with asynchronous reset. The D-FF has three inputs which are "data," "clock," and "reset_bar," and two outputs which are "Q" and "Q_bar." At the rising edge of the clock, the input data transfers to the output Q and it is opposite to Q_bar. While the reset_bar input is asynchronous that does not depend on the rising edge of the clock and its active low "operates at zero." It has the ability to count from "0000" to "1111." The clock inputs of all flip flops are cascaded, and each flip flop's D input (DATA input) is connected to one of the flip flop's state outputs. Each active edge or positive edge of the clock signal will toggle the flip flops. The first flip flop is connected to the clock input. The clock signal is input to the other flip flops in the counter via Q_bar output of the previous flip flop. When the clock signal has a positive edge, the output of the first flip flop will change. Also, the main components to build a D-FF are the 3-input-NAND gate and 2-input-NAND gate as shown in Fig. 12.

Hardware implementation and simulation results

We simulate a five-stage single-ended current-starved VCO oscillator and the reset counter in the 0.13 μm CMOS technology using Cadence virtuoso tools. The simulation results of current-starved VFC, reset counter, and VCO-based ADC are



R	C	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

Fig. 12 Block diagram of the proposed D-FF

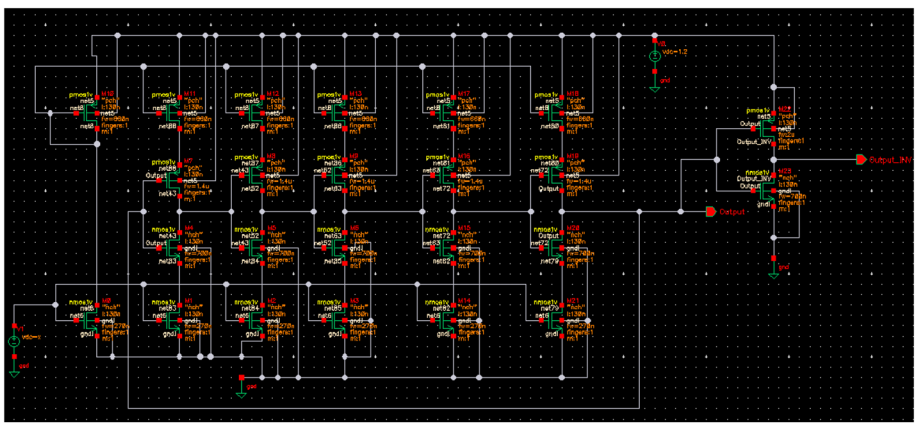


Fig. 13 Proposed current-starved VCO in Cadence virtuoso

demonstrated in Figs. 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, and 28. The circuit schematic of the proposed VCO in Cadence virtuoso is shown in Fig. 13, while the output of current-starved VCO is shown in Fig. 14. The output of VCO is a sine wave whose output frequency is proportional to the input sampled voltage and is converted to frequency modulated pulses by the inverter that placed after the current-starved VCO. The output waveform of the five-stage VCO at 0.4 V input control voltage has an equivalent frequency which is nearly equal to the sampling frequency of 100 MHz.

Figure 15 shows the tuning curve obtained from the simulations of the proposed VFC. The figure demonstrated the input voltage control varying from 0.4 V to 1.2 V

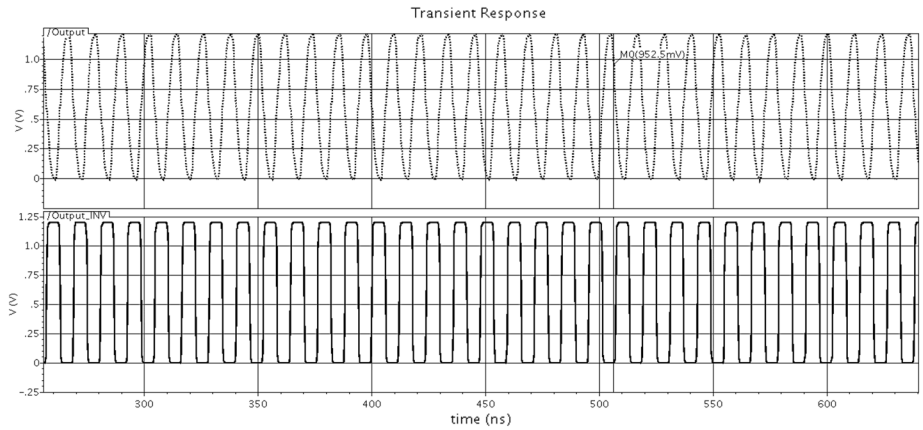


Fig. 14 Output of proposed current-starved VCO, before and after the inverter

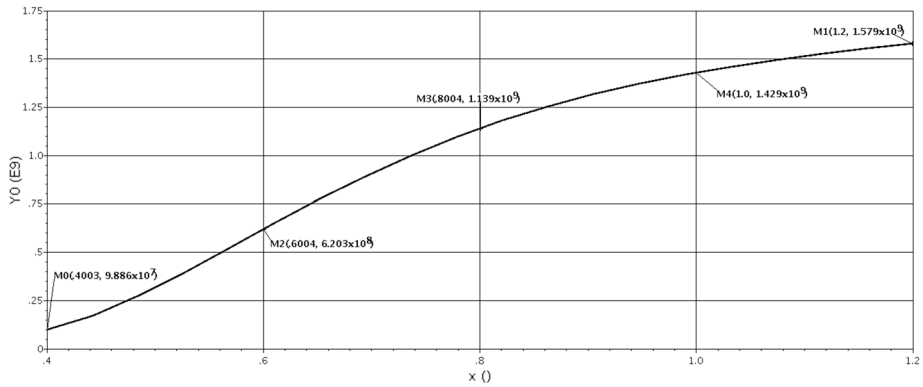


Fig. 15 Voltage-to-frequency tuning curve of proposed current-starved VCO

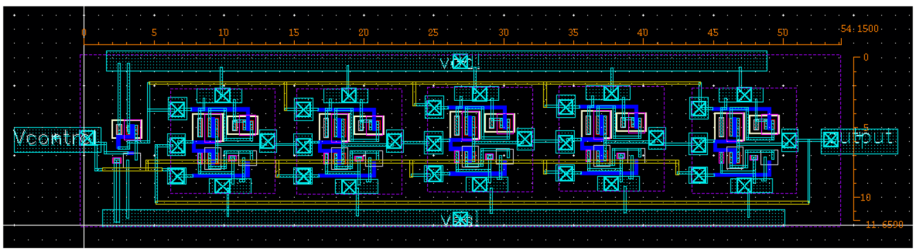


Fig. 16 The layout of the proposed VFC

and the corresponding output frequency varying from almost 100 MHz to 1.6 GHz, respectively. Noted that by adjusting the sizing of the transistors, the minimum frequency equals near to sampling frequency of 100 MHz and the maximum frequency equals near to 16 times the sampling frequency (1.6 GHz) which shows a good resolution for the VCO output. Also a good linearity tuning curve is achieved. The transistors sizing is listed in Table 1. The layout of the proposed VFC is shown in Fig. 16. The active area is 630.85 μm^2.

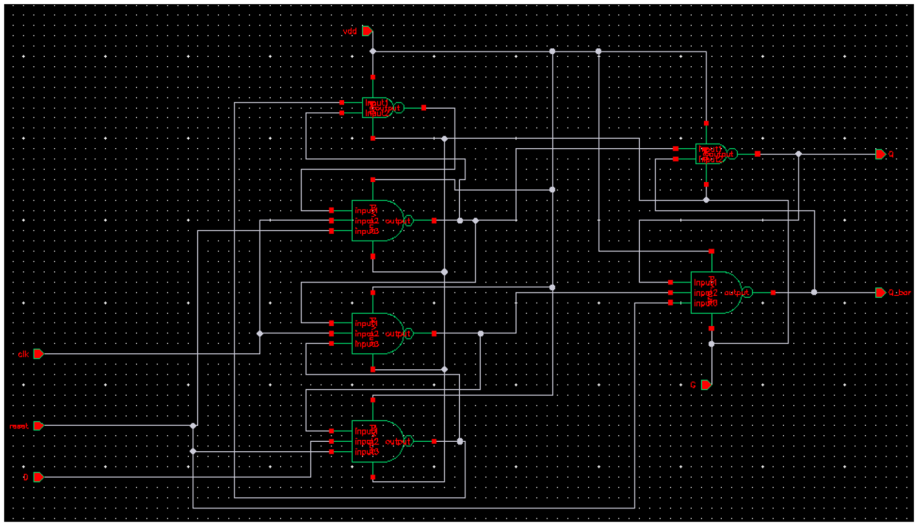


Fig. 17 The D-FF circuit implementation

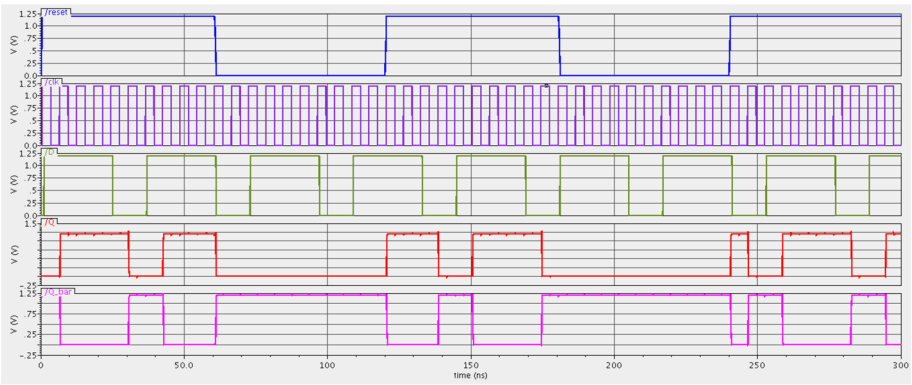


Fig. 18 The timing diagram of the proposed D-FF

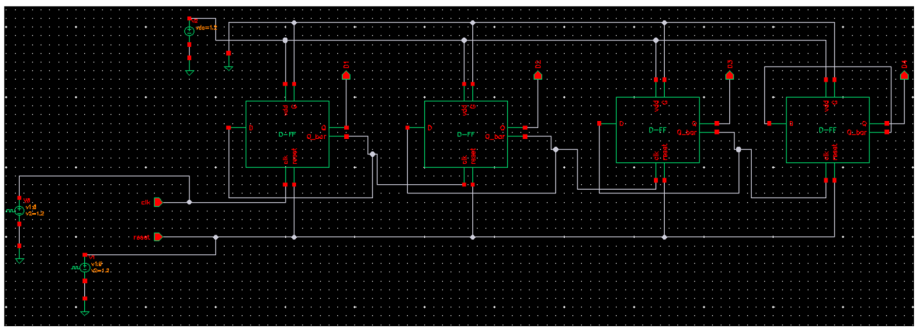


Fig. 19 The reset counter implementation

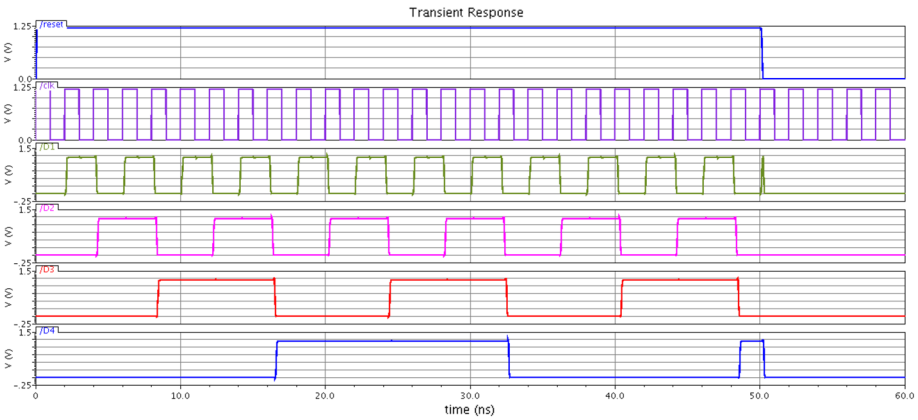


Fig. 20 The timing diagram of the proposed reset counter

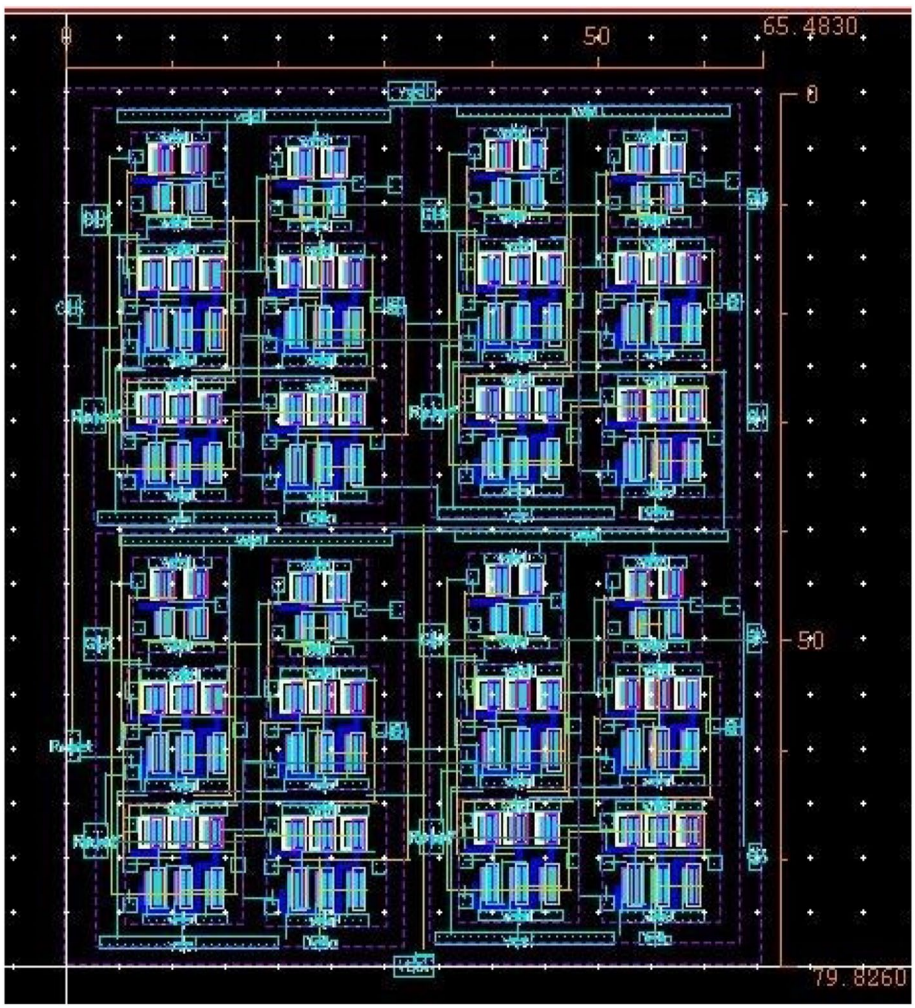


Fig. 21 The layout of the proposed reset counter

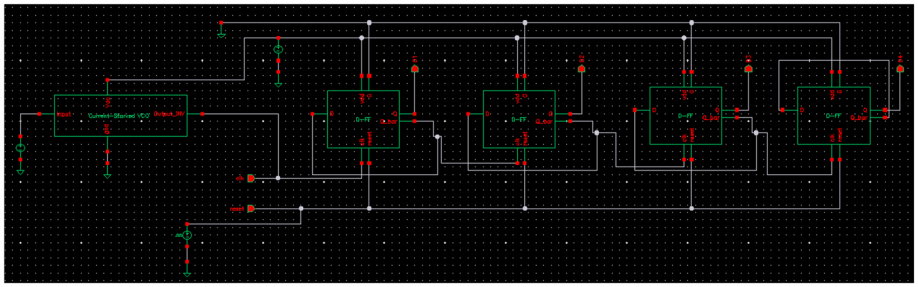


Fig. 22 The schematic of the proposed VCO-based ADC

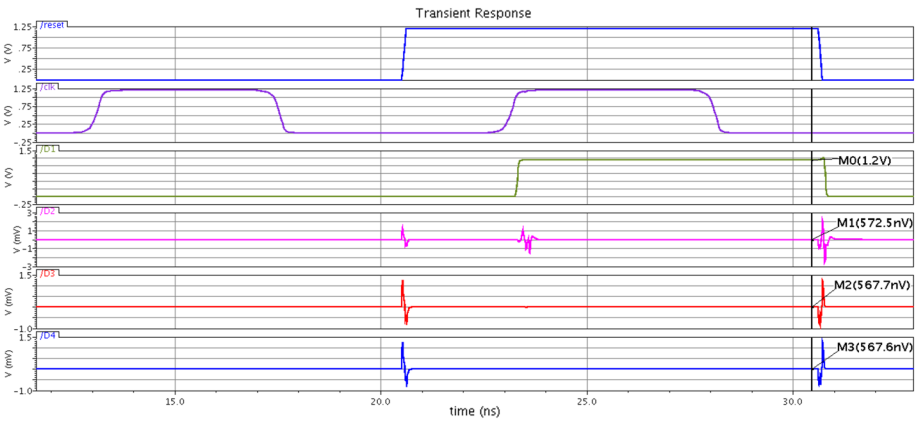


Fig. 23 The output of the VCO-based ADC for 0.4 V input voltage

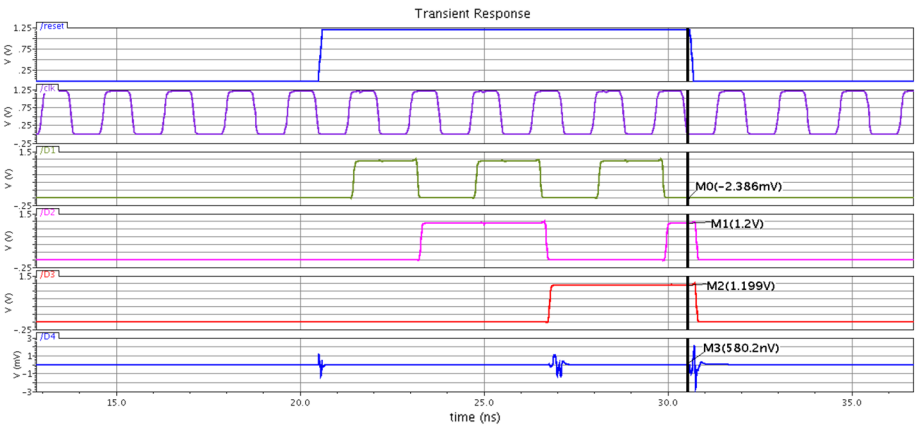


Fig. 24 The output of the VCO-based ADC for 0.6 V input voltage

The D-FF circuit has been implemented by using 3-input & 2-input-NAND gates as shown in Fig. 17. The input data "D" transfers to the output "Q" at each rising edge of the clock as shown in Fig. 18. If the asynchronous reset_bar is set to "0," the output goes to "0," regardless of the rising edge of the clock.

The counter is used to count the number of rising edges (and thus the frequency) that is generated by the VCO for a particular input signal during the sampling clock period.

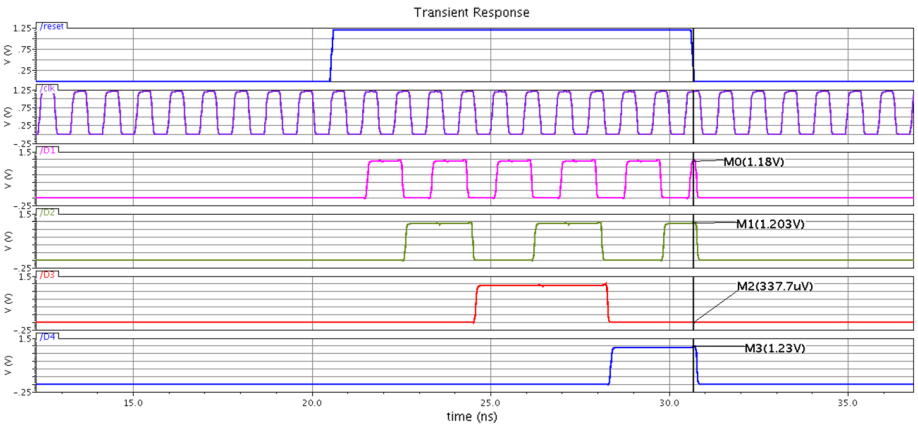


Fig. 25 The output of the VCO-based ADC for 0.8 V input voltage

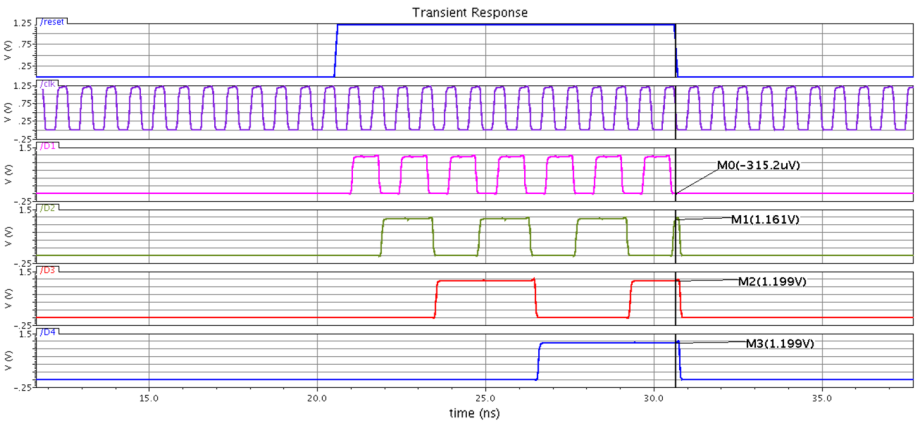


Fig. 26 The output of the VCO-based ADC for 1 V input voltage

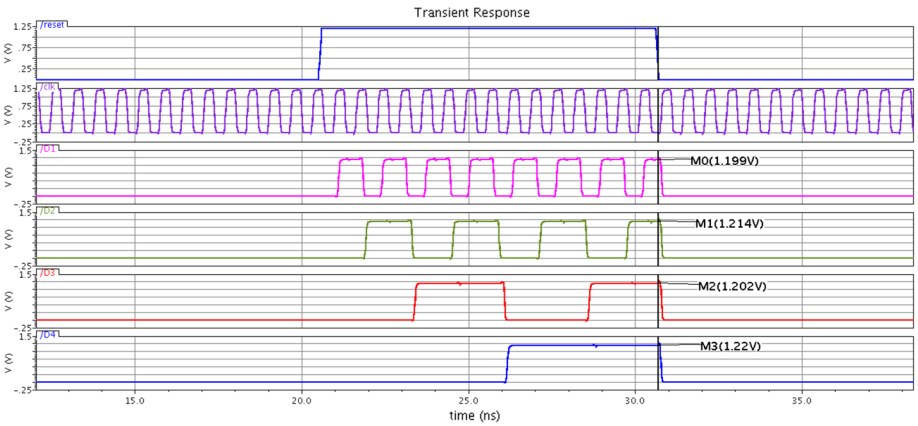


Fig. 27 The output of the VCO-based ADC for 1.2 V input voltage

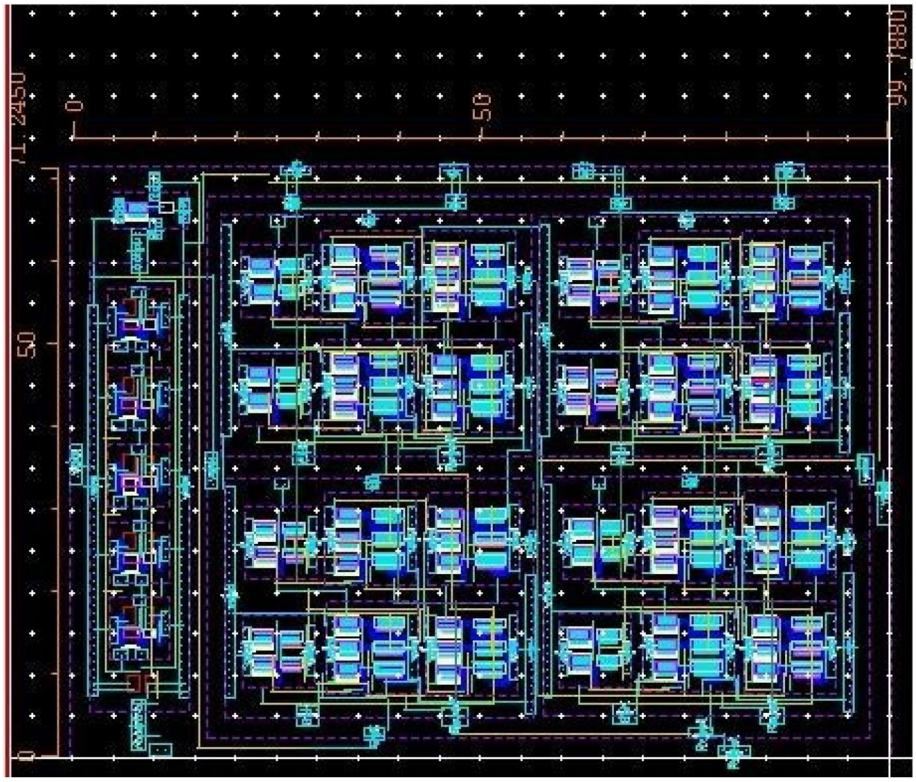


Fig. 28 The layout of the proposed VCO-based ADC

Table 1 Design parameter values of proposed current-starved VCO

	Mn1-Mn6	Mp1-Mp6	Mn7-Mn11	Mp7-Mp11
L (nm)	130	130	130	130
W (nm)	270	660	700	1400

At the end of every period, the counter value is read out by a sampling register and the counter is reset to zero.

The reset counter has been implemented by using four cascaded D-FF as shown in Fig. 19. The four-bit counter counts from 0 up to 15, and whenever the reset_bar is active low the counter returns back to zero as shown in Fig. 20. When the counter reaches counting up till 15 "1111" it returns back to zero and starts counting again. The layout of the proposed reset counter is shown in Fig. 21. The active area is 5227.24 μm^2.

Figure 22 shows the schematic of the proposed VCO-based ADC which consists of the current-starved VCO followed by the reset counter. The output of the VCO-based ADC for different input sampled voltages is shown in Figs. 23, 24, 25, 26, and 27 for 0.4 V, 0.6 V, 0.8 V, 1 V, and 1.2 V, respectively. The corresponding digital output from the VCO-based ADC is "0001," "0110," "1011," "1101," and "1111," respectively. The layout of the proposed VCO-based ADC is shown in Fig. 28. The active area is 0.007 mm^2.

To differentiate the performance of different ADCs, a Walden FoM is used which equals $\mathrm{FoM_W} = \mathrm{P}/2^{\mathrm{ENOB}} \times 2\mathrm{BW}$, where BW is the bandwidth of the input signal to be,

Table 2 Performance comparison of VCO-based ADCs

	Process (nm)	Supply voltage (V)	Sampling rate F_s (MHz)	BW (MHz)	SNDR (dB)	Power (mW)	Area (mm^2)	FoM_W (fJ/step)
[18]	130	1.8	20	0.02	69.6	0.28	0.02	148
[20]	65	1.2	205	2.5	64.2	1	0.06	150.9
[21]	90	1	1000	5	74.1	–	–	–
[15]	180	1.8	400	10	72.6	24	–	360
[23]	130	1.2	2.4	0.02	73.8	0.24	0.04	1499
This work	130	1.2	100	1	62	0.257	0.007	125

ENOB is the effective number of bits of the ADC, and P is the power consumption of the ADC. ENOB is determined from $\text{ENOB} = (\text{SNDR} - 1.76)/6.02$.

The performance of the proposed VCO-based ADC is presented in Table 2. Also, performance comparison of the proposed VCO-based ADC with the state of the art is presented in Table 2. The power consumption of the proposed ADC is 0.257 mW. Low area and less power consumption are accomplished by our ADC. This work achieves a Walden's FoM of 125 dB.

In this paper, a simple implementation of VCO-based ADC comes to exceed the battery lifetime by decreasing the power consumption as compared with previous work which makes it more appropriate for biomedical applications. An efficient current-starved scheme has been proposed to implement the VCO with five-stage and a simple D-flip flop (D-FF) scheme has been proposed to simplify the hardware architecture of the proposed reset counter. Thus, the battery lifetime is exceeded by decreasing the power consumption by 74%. Furthermore, there is a reduction in the area by up to 88% compared to previous works [20] which makes it more appropriate for fully implantable biomedical devices.

Conclusions

We designed an indirect time-based ADC for biomedical applications. The preceding design has been implemented in 130 nm CMOS process. A voltage-to-frequency converter is implemented by using a five-stage current-starved VCO in order to convert the input voltage-to-frequency modulated pulses. Then, a reset counter is implemented to count those pulses and so it converts the frequency varied pulses into a digital code equivalent to the input sampled voltage. The SNDR of the proposed design is 62 dB. Also, our ADC consumes 0.257 mW. This is extremely low power consumption as compared to the state of the art.

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Author contributions
The author has collected data, designed the proposed work, implemented the proposed design, compared the proposed with state of the art, and written, reviewed, and submitted the manuscript.

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Declarations

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