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A comprehensive survey on reduced switch count multilevel inverter topologies and modulation techniques

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Abstract

Multilevel inverters (MLIs) are becoming commonly increasing in high- and medium-power applications. This is because MLI has various intrinsic advantages over conventional two-level inverters, including reduced device ratings, high-quality output, and so on. Most of the traditional topologies are still used in key applications, and there is an increased attentiveness to emerging multilevel topologies to minimize the number of gate drivers, power semiconductor devices, and/or isolated DC sources. Although MLIs have a promising future in industry-oriented applications, their commercial acceptance has been constrained by their size cost, excessive device count, and switch complexity. To convey the drawbacks of MLIs, academics are continually developing next-generation topologies known as reduced switch count (RSC) MLIs. For various reasons throughout the past 10 years, many MLIs with RSC topologies have been described. In this study, an overview of some of the more newly proposed multilevel inverter network topologies that achieve the legitimate goal is presented.

Keywords: Multilevel inverters, Reduced switch topology, Pulse width modulation, Control techniques

Introduction

The exploration and growth of multilevel inverters have significant increase in recent years, though this technology is continuously being researched, developed, and new MLI circuit topologies have just been demonstrated.

The main idea behind a multilevel inverter is to produce a staircase AC voltage waveform with a close sinusoidal shape, by connecting many semiconductors power switches to DC input voltage sources. MLI topologies are gaining attention because they offer lower power ratings for switches. Lower electromagnetic interference and improved harmonics performance may be achieved by producing a staircase voltage waveform with a sinusoidal shape.

The multilayer inverter (MLI) is a power conversion (DC/AC) technology used in power electronics and renewable energy systems. A construction does not require a transformer, switching losses are low, and power semiconductors are less stressed and are the most important characteristics of MLIs.

The MLIs create a stepped output voltage waveform by aggregating numerous tiny voltage levels; this solution is effective for medium-voltage and high-power applications. MLIs have several advantages, including lesser stress on switches, reduced total harmonic distortion (THD), lower di/dt, lesser dv/dt, and low electromagnetic interference (EMI). Consequently, MLIs have stood up to be a mature technology for many custom and commercial products for an extensive variety of power applications particularly flexible alternating current transmission systems (FACTS), high-voltage direct current (HVDC) transmission, battery energy storage systems (BESS), adjustable speed drives (ASD), custom power devices (CPD), electric cars (EV), active frontend converters (AFC), and renewable energy generation (REG). MLI has some disadvantages; the most notable of which is its harmonic problem, which has negative consequences for certain applications, e.g., reduced lifespan of the system, production of torque pulsation in electric drives, and degrade efficiency.

Multilevel inverters have been designed and meant for higher voltage levels. The most common and familiar multilevel inverter designs are: "Diode clamped (DCMLI)" [1], "Flying capacitor (FCMLI)" [2], and "Cascaded H-bridge (CHB)" [3] as shown in Fig. 2. Although these topologies have received significant interest from both academia and industry, their actual application is significantly inclined by the switch intricacy, cost, and application.

Diode-clamped MLIs are classified into three types: basic, enhanced, and modified. The improved version has numerous advantages. The flying-capacitor type employs capacitors rather than clamping diodes, and its performance is comparable to that of diode-clamped inverters. The cascade type is made up of half-bridge inverters, and the output waveforms are of higher quality than those of other varieties. Each half-bridge, however, requires its DC supply. The cascaded inverter is distinct from the diode-clamp or flying-capacitor inverters, as it does not need any of the voltage-clamping diodes or voltage-balancing capacitors as mentioned in Table 1.

Cascaded multilevel inverters achieve higher voltage and power levels (MLI) and are shown to be more adaptable than traditional topologies. Its modularity can be leveraged to boost the performance of the inverter's power output. Cascaded MLIs are built by linking the output terminals of numerous H-bridges in sequence as a result, and it is clear that this configuration allows for high power levels while using a low voltage rating components found in inverters. In the event of a fault in any of them, it is simple and quick to change the inverter cells as a result of its modularity (Figs. 1, 2 and 3 and Table 1).

Topologies of reduced switch count multilevel inverters

The concept of minimizing the number of switches in inverters was first proposed in 1996 when a low-power bilateral DC-link inverter with overall eight switches was suggested for motor driving applications [4]. The continual growth based on high-concert power semiconductor devices has prompted the development of many other inverter research trends as shown in Fig. 1. As a result, researchers proceeded to experiment with and evolve fresh topologies by modifying traditional MLIs in various ways as shown in Fig. 3. As a result, asymmetrical CHB designs are advantageous in reducing the switch

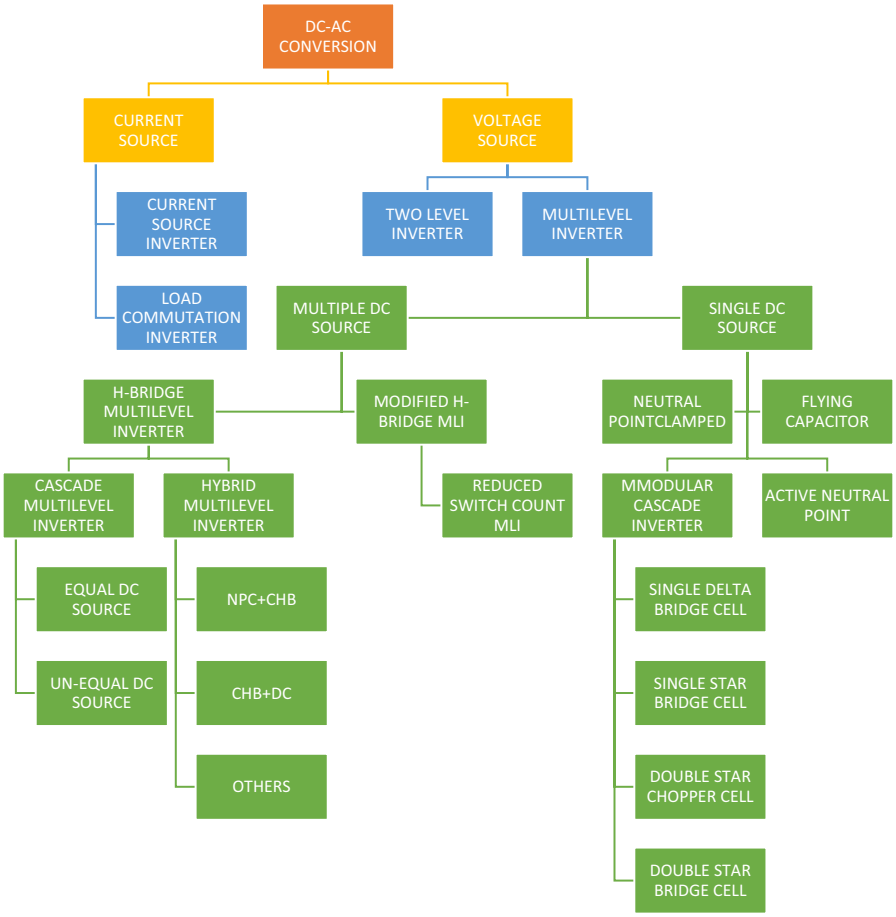

Fig. 1 Evolution of MLIs

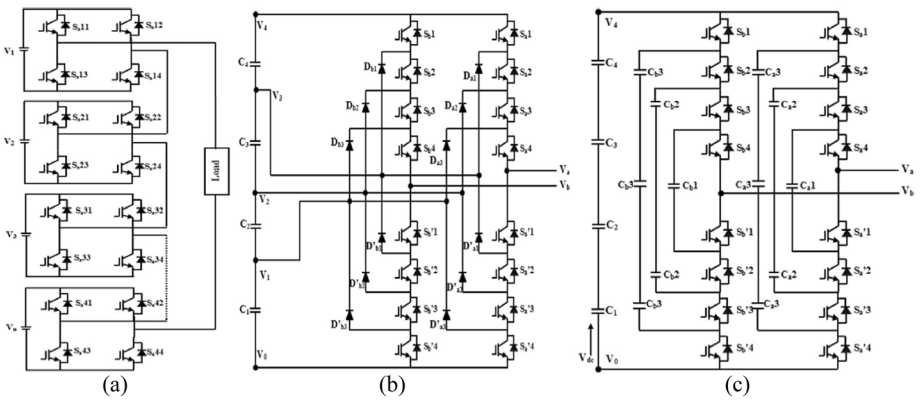

Fig. 2 1-φ conventional MLIs **a** cascade H-bridge (CHB), **b** neutral point clamped (NPC) and **c** flying capacitor (FC)

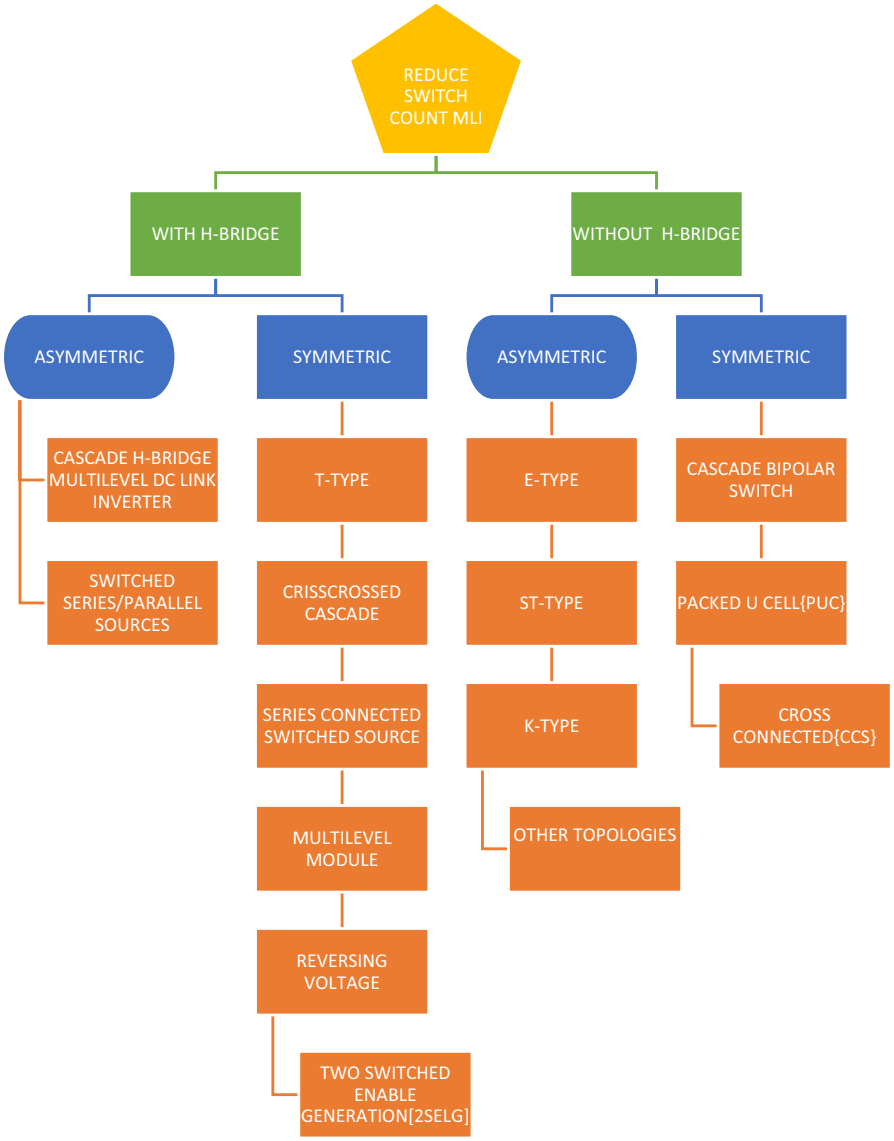

Fig. 3 Topologies of reduced switch count multilevel inverters

Table 1 Comparisons of component necessities per leg of three multilevel converters

Type of MLI	No. of DC source	DC-bus capacitors	No. of switches	Clamping capacitors	Clamping diodes
Diode clamped	1	$m-1$	$(m-1)*2$	0	$(m-1)*(m-2)$
Flying capacitor	1	$m-1$	$(m-1)*2$	$(m-1)*(m-2)/2$	0
Cascaded H-bridge	$m-1/2$	–	$(m-1)*2$	0	0

count so that they can increase the number of levels [3] and further enhance configurations for refining the performance of conventional MLIs appeared.

Cascaded MLIs structures have also gained courtesy due to superiority over earlier topologies, for example, the non-existence of diodes and capacitors despite producing increased levels in high-power applications and a simpler control structure. New multilayer inverter architectures, such as asymmetrical cascaded multilevel structures and hybrid structures, have newly emerged to abate the quantity of input DC voltage sources [5]. Yet, certain algorithms are required for these structures to compute the number of voltage sources. Furthermore, having surplus switches is not cost-effective.

To enhance the number of levels, asymmetrical CHB multilevel inverter (CHB-MLI) topologies came into existence by linking dissimilar un-equal DC voltage sources. The primary downside is that the stresses on the switches are not equivalent. Switches associated with the maximum input DC voltage have more voltage stress when compared to switches associated with the minimum input DC voltage. Switch temperatures will vary because of unbalanced loss sharing among switches. Furthermore, differential voltage stresses necessitate the employment of separate voltage ratings for switches, resulting in a higher cost; nevertheless, the benefits of the CHB, such as simplicity, simple control, modest structure, and adaptability, have been overlooked.

Su et al., [6] showed the architecture, which involves multilevel DC-links (MLDCL) at the CHB inverter. MLDCL inverter with three DC input sources is shown in Fig. 4. The circuit comprises "n" half-bridge units combined in series, individually with two switches and only a DC source. These series-connected units, also known as level-generation parts, enable the development of a stepped DC voltage waveform. By altering the output voltage's polarity, the H-bridge can yield a complete multilevel AC waveform. With fewer semiconductor switches, using the MLDCL topology, the output voltage level can be produced. Dc-bus voltage of staircase-shaped steps is provided by the MLDCL created by the half-bridge cells to the single-phase full-bridge inverter, which then alternates the voltage polarity to create an AC voltage with $(2^{*}n+1)$ levels.

$$V_{\text{bus}} = |\upsilon_{\text{an}}|$$
$$i_{\text{bus}} = \begin{cases} i_{\text{a}}, & \text{for} \quad \upsilon_{\text{an}} \geq 0. \\ -i_{\text{a}}, & \text{for} \quad \upsilon_{\text{an}} < 0. \end{cases} \tag{1}$$

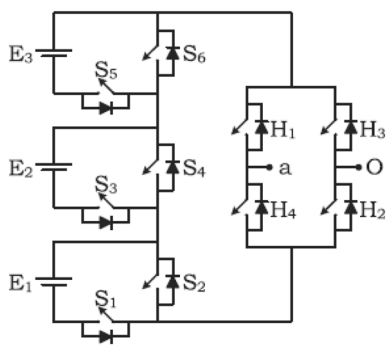

Fig. 4 Multiple-level DC-link inverter (MLDC)

The peak fundamental component of the AC output can be determined by

$$\upsilon_{\text{an\_1}}(\text{peak}) = -\sum_{k=1}^{n} V_{sk} \sin \frac{\theta_k}{2} \tag{2}$$

Prasad et al. [7] proposed a new way of optimizing Dstatcom's DC-link voltage by employing RSC-MLI with a photovoltaic panel as a source of input. The Perturb and Observation (P&O) algorithm is implemented to accomplish MPPT. To produce the gate pulse for Dstatcom, ISCT (instantaneous symmetrical component theory) is used. PV panels can efficiently balance the load during the day, produce real power, and operate as a Dstatcom during the night to improve the power quality. The proposed method's outputs are capable of successfully adjusting reactive power while lowering harmonic content. The percentage of THD is significantly reduced after compensation and regulation of the DC-link voltage.

The SSPS-MLI topology was put forth by Hinago and Koizumi [8]. It consists of two main components, one "level-generation" part (that produces a positive polarity staircase voltage waveform) and the other "polarity-generation" part (which transforms the waveform of the staircase DC voltage to AC voltage), as shown in Fig. 5. In comparison with other typical MLI topologies, this configuration has the advantage of being able to yield extra output voltage levels with fewer quantity switches. Solitary firm DC-link voltage is adequate for all of the DC-link capacitors to charge. Once the SSPS enters self-balancing mode, the level count and output voltage increase. This SSPS function is ideal for applications involving battery charging and energy storage [9]. Li et al. [10] suggested a reduced series/parallel module (RSPM) designed as cascaded ML-STATCOMs. In comparison with traditional H-bridge modules, in RSPM, the added switch permits parallel connectivity; in addition, cycling the parallel state across the arm ensures sensorless balance. When compared to current methods, the proposed solution requires 25% fewer transistors.

Ceglia et al. [11] were the first to suggest a unique T-type arrangement with a 5L single-phase inverter. The key advantage is that the intended configuration eliminates the requirement of additional switches. Figure 6 shows the topology of a T-type inverter, and Fig. 7 represents the output voltage of T-type inverter. When compared to other existing topologies, T-type topology provides a significant improvement in terms of switch count and layout complexity. Furthermore, without diodes or

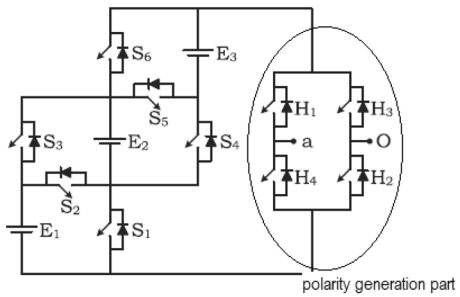

Fig. 5 Switched series/parallel sources MLI

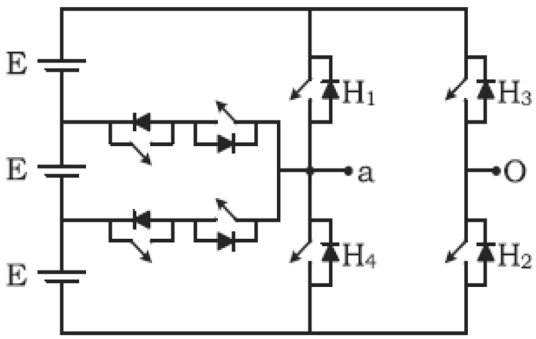

Fig. 6 T-type multilevel inverter

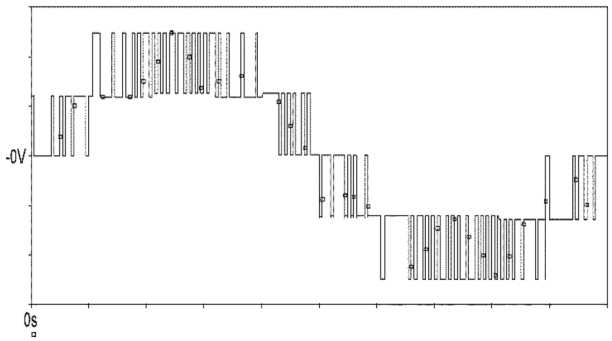

Fig. 7 Simulated five-level converter output voltage

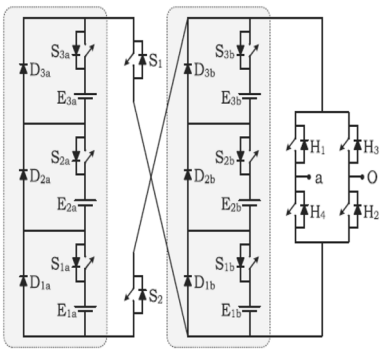

Fig. 8 Crisscross cascaded MLI

capacitors, the power switch count is reduced by nearly 40–50% [12]. This arrangement includes an auxiliary bidirectional switch and H-bridge for managing the supply linking through DC sources to produce a staircase output voltage. But, unlike asymmetric H-bridge topologies [11], this architecture fails to render switching states with all required levels.

Khosroshahi presented a CCHB-MLI architecture with cascaded basic units in [13]. Figure 8 depicts a CCHB inverter arrangement with a mix of unilateral and bilateral switches and three DC voltage sources. It consists of two components: the level-generation component and the polarity-generation component. The level-generation

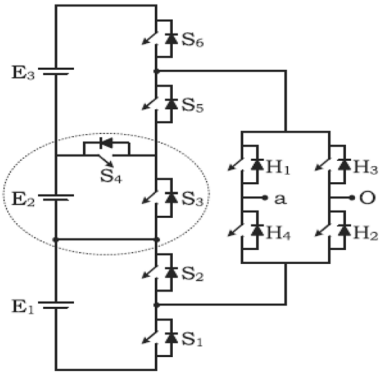

Fig. 9 Reversing voltage MLI (RV-MLI)

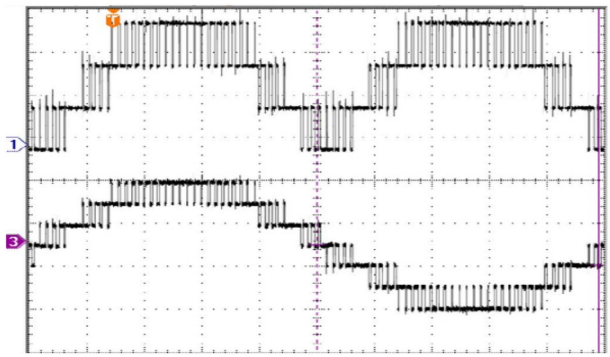

Fig. 10 Output waveforms in the proposed topology

component features two unidirectional power switches, namely Sw_2 and Sw_3. Sw_4 and Sw_1 are bidirectional blocking and conducting switches, respectively. P1, P2, P3, and P4 are the four power switches that make up the polarity-generation component. CCS requires $(2n+6)$ switches and obtains $(4n+1)$ levels. Advantages of this presented topology include: (i) the use of fewer semiconductor switches; (ii) the bounded utilization of separate voltage DC sources when related to other traditional topologies, and (iii) lower volume and cost than CHB-MLI [14].

Najafi et al., initial's proposal for voltage reversal for MLI topology can be found in [15, 16]. Both the level-generation part and the polarity-generation part in this design generate the sinusoidal output voltage. According to Fig. 9, voltages with positive and negative polarity are produced, respectively. Figure 10 shows the output voltage of RV-MLI by the level-generation and polarity production stages. The application to three stages can easily be expanded by replicating the middle stage process through a slight number of levels. It has flexibility in the switching order and requires a minimal number of components to function. As a result, it may be helpful for applications like FACTS and HVDC. In this architecture, however, the matter is reasonably difficult to associate add-on and deduct DC sources; operation via separate DC sources is not feasible herein architecture.

The key notion in this architecture is the series joining of sources through the switches [17]. Figure 11 depicts an MLI configuration based on SCSS. In this case, semiconductors

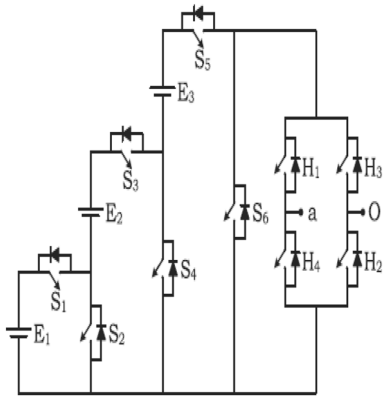

Fig. 11 Series-connected switched sources multilevel inverter (SCSS-MLI)

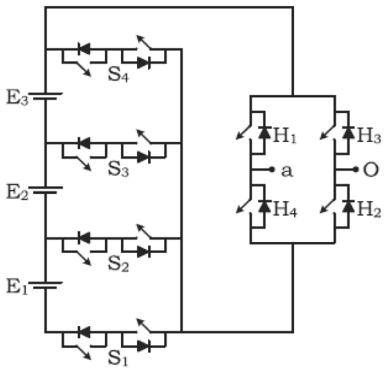

Fig. 12 Multilevel module-based multilevel inverter (MM-MLI)

are paired with the smaller magnitude poles of the voltage sources. Additionally, they are in touch with the stronger voltage poles of the upstream source. Through the help of the H-bridge, the connection can generate a DC voltage with different levels that yield into consideration of mutual polarities. This construction also aids in lessening the number of switches essential for the inverter's symmetrical structure.

Multilevel module MLI topology that consist of the level-generation component along with the polarity-generation unit was proposed by Babaei in [18]. An MLM multilevel inverter with three input DC sources is shown in Fig. 12. This arrangement can function with fewer semiconductor switches, transistors, and power diodes due to the increased level of output voltage. As it cannot be employed in an asymmetric form, this is its main drawback. Despite that it can remain beneficial for larger power quality applications utilizing a range of DC voltage sources [18].

Tanaka et al., [19] discuss the STATCOM performances of four configurations of the modular multilevel cascade converter family including SSBC, DSCC, SDBC, and DSBC over large-scale offshore wind power plants, in conjunction with an emphasis on the possibility for asymmetrical low voltage ride through (LVRT) grid disturbances. In this literature, due to DC-link capacitor voltage management and voltage-stabilize control procedures for converter cells, namely the zero-sequence AC

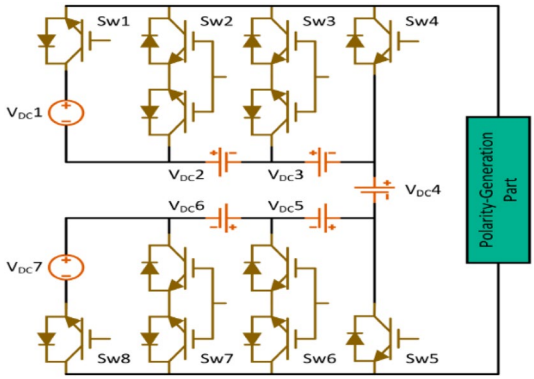

Fig. 13 Two-switch-enabled level generator-based multilevel inverter (2SELG-MLI)

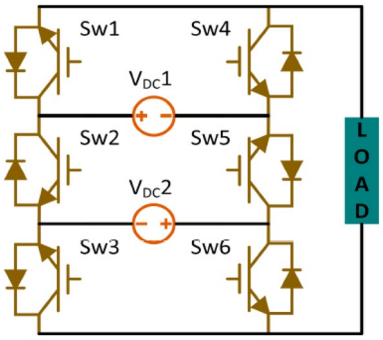

Fig. 14 Cross-connected source-based multilevel inverter (CCS-MLI)

injection method for SDBC along with zero-sequence AC voltage injection method despite SSBC, practical designed SDBC and SSBC have non-availability LVRT working situations underneath fewer grid failure scenarios. By engaging the voltage-balancing control with circulating two-degree DC, DSCC and DSBC can maintain operation in all circumstances without any current derating.

Figure 13 illustrates the level of production-based MLI topology that Babaei found in [20]. It has two switches and seven input levels. Level generation and polarity generation are the two distinct steps in this structure. The name "Two Switch" explains that this arrangement can synthesize any level of voltage with only two conducting switches in the level production step. However, under asymmetric topology, this inverter is unable to function. The main drawback is that using a fundamental switching frequency, it will be difficult for the level production step and isunsuccessful to understand the zero level on its own [21].

Authors of [22] proposed the cross-connected source MLI topology, which has DC input sources segregated for each cell, as shown in Fig. 14. The two terminals of two separate sources in this architecture are connected to a switch and vice versa. When isolated DC sources are provided, it normally activates with a small number of switches [14]. The output voltage of five-level CCS-MLI is shown in Fig. 15, Harmonic order is shown in Fig. 16.

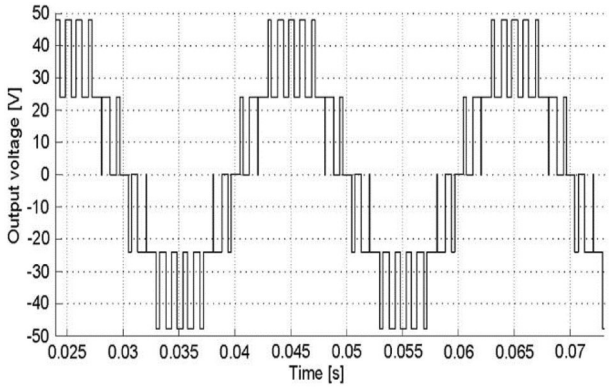

Fig. 15 Five-level output voltage of CCS-MLI

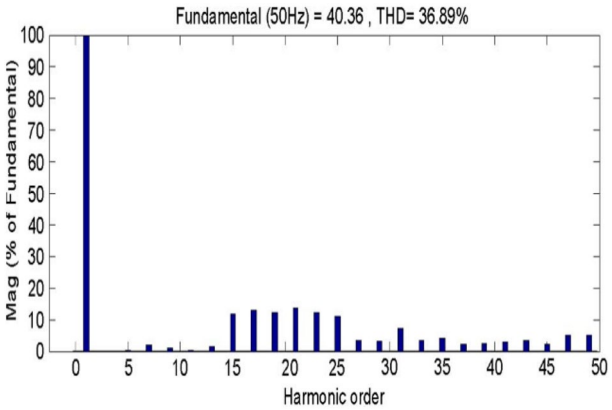

Fig. 16 Harmonic spectrum of the load voltage

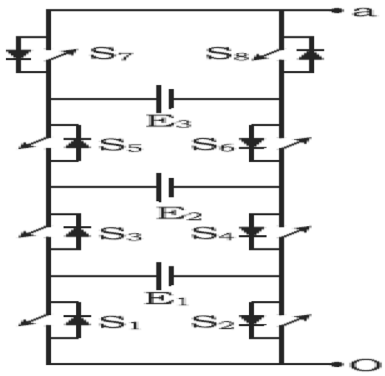

Fig. 17 Packed U-cell multilevel inverter (PUC-MLI)

Ounejjar et al. [23] proposed the "PUC" topology, a novel MLI topology. Figure 17 shows the PUC-MLI circuit that comprises of four direct current sources and ten power semiconductor switches. Each U-cell includes two switching units in addition to a single DC input level [21]. The primary benefit of this technology is the ability to run the extreme voltage-producing switch at the lowermost frequency. Additionally,

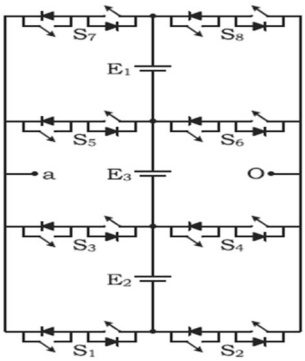

Fig. 18 Cascaded bipolar switched cells multilevel inverter (CBSC-MLI)

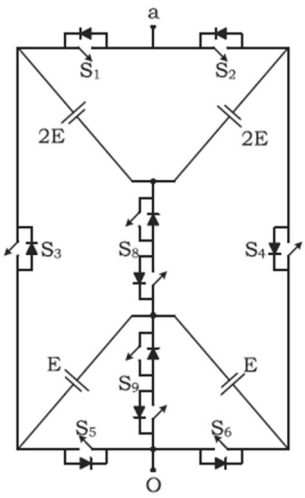

Fig. 19 E-type MLI

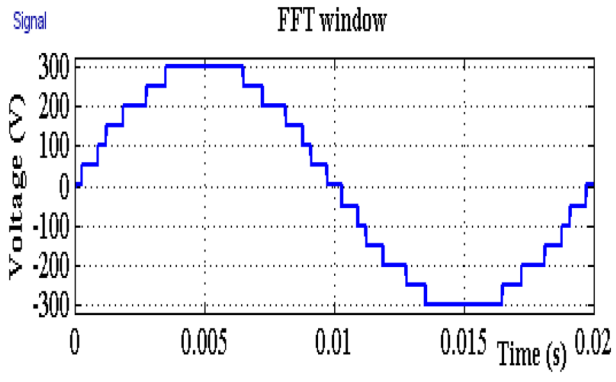

Fig. 20 Output voltage of 13-level E-type MLI

it makes changing the voltage level significantly simple, puts less strain on the switch, and advances the performance of the converter as a whole.

The circuit network, shown in Fig. 18, was first presented by Babaei et al. in [24]. Eight bilateral power semiconductor switches in the circuit, combined with three DC

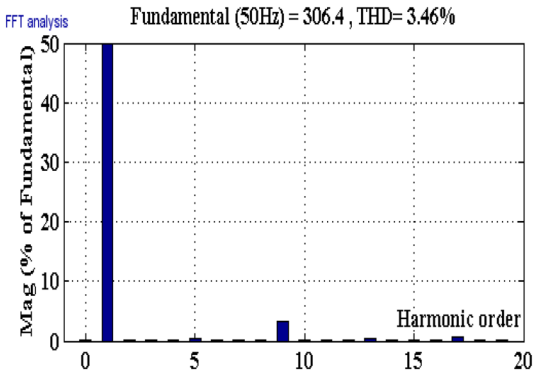

Fig. 21 Harmonic order of 13-level E-type MLI

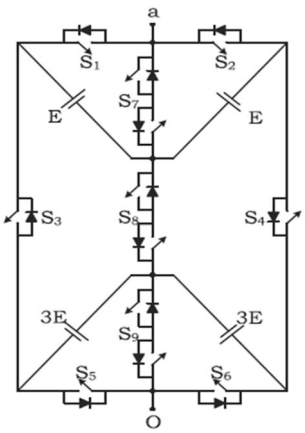

Fig. 22 Square T-type (ST-type)

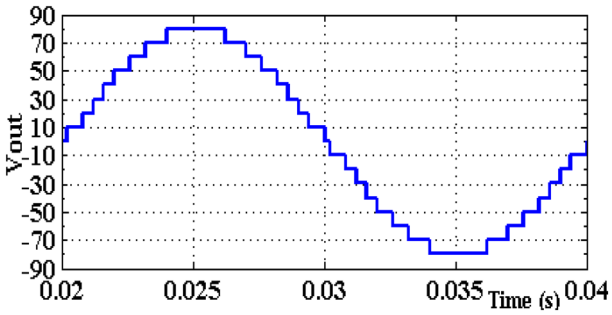

Fig. 23 Output voltage of 17L ST-type MLI

sources, provide voltage levels with a positive and negative polarity. There are exactly as many gate drive circuits as there are bidirectional switches, which each require two IGBTs. This idea aids in reducing the circuit's overall complexity and operational costs. This topology's primary drawback is that it is incompatible with asymmetric configurations.

The E-type module [25], shown in Fig. 19, is a 13-level inverter with six unidirectional and two bidirectional switches placed in a wrapped structure, as well as four

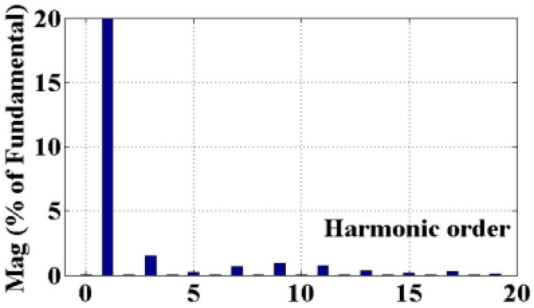

Fig. 24 Harmonic order of 17L ST-type MLI

DC sources with a voltage ratio of 1: 2. The output voltage and harmonic analysis is shown in Figs. 20 and 21. The square T-type (ST-type) was modeled after the E-type, whose individual primary unit behaves as a 17L inverter as shown in Fig. 22 [26]. Six unidirectional switches, with a 1: 3 voltage ratio of four DC voltages, and three bidirectional switches structure the ST-fundamental-type's unit. This architecture is elevated to bigger levels through cascade/series connections, much like the E-type. Both of these topologies have constrained switching redundancies and uneven device blocking voltages. The output voltage is shown in Fig. 23, and FFT analysis is shown in Fig. 24. A K-type architecture for 13 levels is given in [27], which is similar to an E-type topology except those capacitors which are used in place of the DC sources E2 and E4 in Fig. 19.

Panda et al. [28] introduced a generalized cascaded multilevel inverter topology that operates in both symmetric and asymmetric modes to minimize harmonics. SHE and sinusoidal pulse width modulation (SPWM) approaches are utilized to suppress both lower and higher-order harmonics, and the flower pollination algorithm is used to determine the optimal angles for MLI. When the results of the PSO, TLBO, and CSA techniques are compared to FPA, it is discovered that FPA has quite a faster track to optimal solutions, fewer difficult compilations, and excellent accuracy. Varghese et al. [29] introduce a novel 27-level multilevel inverter topology through a minimal amount of switches. It employs three DC power sources and 13 switches. The aim is to reduce the output total harmonic distortion by analyzing the harmonic spectrum with low-frequency switching techniques and optimizing the switching angles with a fuzzy logic controller. This THD is decreased to 5% when compared to typical methods, and for switching angles (CORDIC), coordinate rotational computer technique is employed.

Siddique et al., [30] propose a new single-phase cascaded MLI topology. The proposed MLI topology is intended to decrease the DC voltage sources with modularization and switch count though maintaining an output with an excess number of levels. Three distinct approaches are proposed for finding the total amount of DC voltage sources and the number of levels in a cascade connection. SHE PWM technique is implemented to suppress lower-order harmonics up to 11th order. The projected topology generates 11-level output with eight switches and three DC sources. Alexander Stonier et al. [31] presented a solar-fed cascade 15-level inverter to handle harmonics in solar PV energy conversion and power quality issues using PI, ANN,

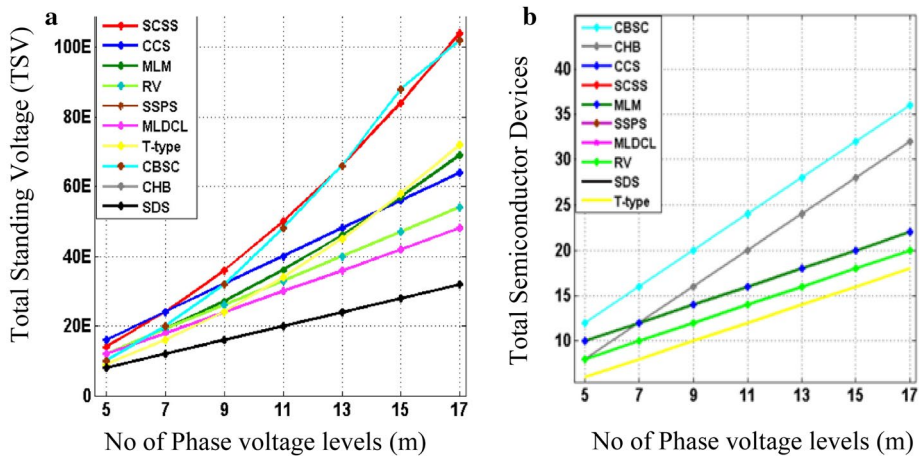

Fig. 25 **a** Comparison of total standing voltage with no. of phase voltages levels (m) of RDC-MLI. **b** comparison of total semiconductor devices with no. of phase voltages levels (m) of RDC-MLI

and fuzzy logic control techniques. When compared to the other two techniques, the fuzzy logic controller produces better performance for voltage regulation, while taking into consideration variations in input solar PV power quality. Comparison of total standing voltage and total semiconductor count in all reduced multilevel inverter is shown in Fig. 25a and b and also comparison of different MLI's merits and demerits are mentioned in Table 2.

MLI control and modulation schemes

The inverters' modulation techniques are essential since they have a direct influence on the overall system efficiency. In MLI, various modulation approaches have been put forth. It is employed to modulate the output current along with voltage as well as to compute two crucial MLI metrics, % THD and switching losses. The goal of a modulation signal is to create a stepped waveform that is the most accurate representation of a certain reference signal feasible. This waveform will include fluctuations in frequency and amplitude as well as an essential component that is normally sinusoidal in a stable state. The graphic representation of general modulation techniques is shown in Fig. 26. The following are the most crucial criteria used to select a specific modulation strategy for a given MLI family: distortion level, total harmonics produced, switching frequency, amount of losses, and response time are among the other metrics.

High switching frequency [HSF] and fundamental switching frequency are the main two types of modulation techniques employed in multilevel inverters. In contrast to HSF, which has numerous commutations for each cycle, fundamental switching frequency only takes one or two commutations per cycle [32]. The two main forms that fall within the category of high switching frequency are pulse width modulation [PWM] and space vector modulation (SVM). Detailed discussions of low and HSF kinds are provided in the section that follows.

Table 2 Comparisons different multilevel inverter topologies

References	No of Switches	Techniques implemented	Symmetrical/ asymmetrical/ both	Merits	Demerits
MLDC [6]	$m+3$	PWM switching angle	Both	Makes use of fewer semiconductor switches Optimum circuit design There is no need for additional clamping diodes or capacitors	Expenses are high since storage capacitors are used Reduced device count causes a rise in power rating, which damages the device
SSPS [8]	$2n+4$(U)	PD-SPWM	Both	Uncomplicated design It is feasible to distribute loads uniformly Able to run as a single DC source configuration Requires fewer gate driver circuits	Inapplicable to fault-tolerant operations and unable to function as an asymmetric configuration
T-type [11]	4(U), $n-1$(B)	FPGA	Symmetrical	The supervised structure is straightforward Diodes and capacitors are not necessary	Switching losses are substantial Low efficiency is the outcome of a high-frequency operation Cannot be used for applications requiring high voltage and/or power
Crisscross [13]	$3n+4$	Vertical-phase-shifted SPWM strategy	Both	The system has low PIV The capacity to function with both negative and positive voltage	Switches that can operate in both directions are necessary Operation requires an isolated input DC-link
RV [15]	$2n+4$(U)	PD-SPWM	Both	DC-links that are not isolated are used Peak voltage and switching frequency are used to operate rated switches	Non-uniform load sharing Low levels of redundancy
SCSS [17]	$2n+4$(U)	PWM switching angle	Symmetrical	A flexible framework Maximum voltage and switching frequency are supported by rated switches	Each switch has a different rating of voltage, which results in uneven load sharing
MLM [18]	4(U), $n+1$(B)	Fundamental frequency switching technique	Symmetrical	Can function with fewer DC source voltages Needs smaller amount of power diodes, transistors, and semiconductor switches	Flops when used in an asymmetrical arrangement Separate DC sources are necessary

Table 2 (continued)

References	No of Switches	Techniques implemented	Symmetrical/ asymmetrical/ both	Merits	Demerits
2SELG [20]	$2n+4$	Staircase control method	Symmetrical	Only a few switches are required Uncomplicated structure	Does not work at the basic switching frequency Intricate control Needs separate DC sources
Cross-connected [22]	$2n+2$(U)	Multicarrier PWM scheme	Both	Need fewer switching devices and fundamental sub-inverter cells For a specific level, it requires the least blocking voltage	Only works with solitary DC sources A need for on-state switches Not very economical
PUC [23]	$2n+2$(U)	Sinusoidal PWM modulator	Both	The architecture is straightforward The potential for further crossover switches	Various switches have varying voltage ratings Applications that can tolerate errors cannot exist Implementation expenses are higher
CBSC [24]	$2n+2$(B)	Fundamental frequency switching technique	Both	Decreased operating costs Basic circuit	Not possible to use asymmetric topology
E-type [25]	6*n*(U), 2n(B)	Selective harmonics pulse width modulation	Asymmetrical	Absolute asymmetry Switching redundancies are produced through cascading	Significant device decrease Voltage balancing with DC-link is challenging
ST-type [26]	6*n*(U), 3n(B)	Nearest level control	Asymmetrical	Switch count is lower than for the E-type	Notable device reduction

Selective harmonic elimination technique [SHE]

Patel [33] created the SHE technique for inverters in 1964 on the way to getting rid of the specified harmonic content order. By using switching angles, the SHE method's primary goal is to decrease the lower-order harmonics inside permissible bounds. The set of nonlinear transcendental equations calculates the switching angles. The foremost task is to solve nonlinear equations while selecting the best approaches or techniques built over waveform formulation, like half-wave symmetric, quarter-wave symmetric, non-symmetric, non-equal, and varying levels. Each sort of waveform's theoretical analysis is provided in [34]. The MLI output voltage waveform often consists of several steps; in addition, it has the nature of a quarter-wave.

Theoretically, the output voltage waveform is analyzed using the Fourier series. Below is a phase voltage Fourier series expression.

$$V(t) = \Sigma V \underset{n=1,3\ldots\infty}{\sin} n(\omega t)\, s \tag{3}$$

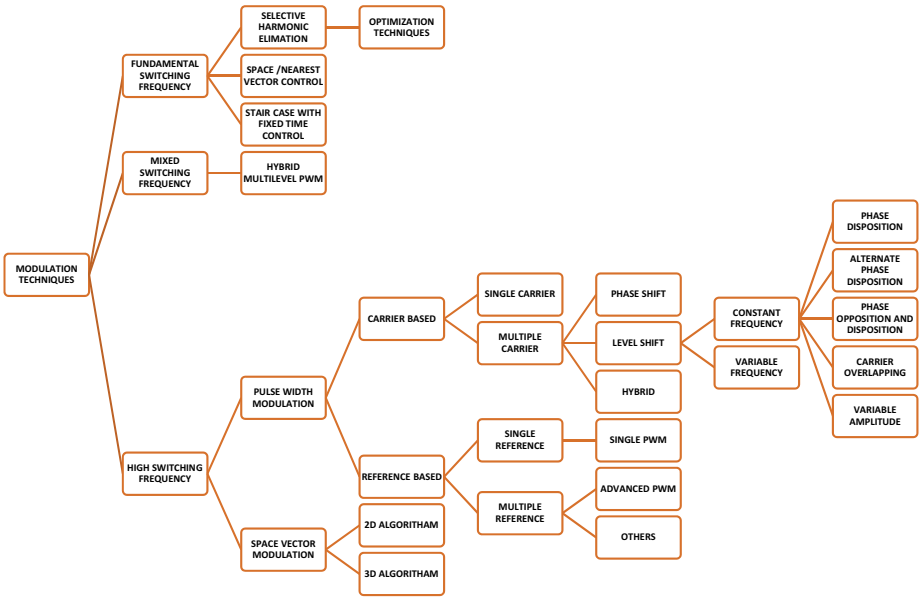

Fig. 26 Pictorial representation of modulation technique

In this case, the primary switching frequency ω, and the magnitude of the nth-order harmonics, Vn, are both represented. One way to express the Vn is as follows:

$$\mathrm{Vn} = \begin{cases} \frac{4V_{\mathrm{dc}}}{n\pi}[\cos(n\alpha 1) + \cos(n\alpha 2) + \ldots + \cos(n\alpha m) & \text{for Odd} \\ 0 & \text{for even} \end{cases} \quad (4)$$

In the above equation, the switching angle (α_{m}) and magnitude of a voltage source (V_{dc}) regarding output voltage waveform are restricted between 0° and $\frac{\pi}{2}$. Therefore, the switching angle margins are perhaps calculated by the expression mentioned below.

$$0 < \alpha_1 \leq \alpha_2 \ldots \leq \alpha_{\mathrm{m}} < \frac{\pi}{2}$$

In addition to removing low-order harmonic components, the SHE technique keeps the waveform's fundamental component intact. This method's primary goal is to reduce switching losses. The SHE approach is utilized for three distinct purposes, including harmonic mitigation, THD minimization, and individual harmonic reduction. The low switching frequency used by SHEPWM techniques indicates that the higher rate of each low-order harmonic element imposed by grid codes or the electrical supplier is not limited.

Optimization techniques

Recently, numerous harmonic elimination strategies based on algorithms have been used in MLI. These techniques transform the transcendental equation into the cost function. Constraints are used to describe the limitation of switching angles. Algorithms are used to determine the switching angle, while the price function is minimalized under the given limitations. In [35], the harmonic profile in RS-MLI is improved using a genetic

algorithm (GA). In [36], to improve the harmonic profile and regulate output voltage, particle swarm optimization (PSO) algorithm was implemented.

For controlling the linearity of the switching angle total harmonic distortion, in asymmetric cascaded MLI, PSO can be used [37]. In 3-ϕ inverters with unipolar output voltage waveforms, the harmonic content is removed using the ant colony system (ACS) [38]. In [39], the seven-level CHB-MLI algorithm uses the bee algorithm (BA). Compared to the GA approach, this method offers higher convergence. When compared to GA, it offers some benefits such as precision, faster speed, and convergence power.

A three-phase inverter uses a clonal search algorithm (CSA) [40]. Through the variable amplitude of the initial component, this technique is employed to produce the triggering angle and related waveforms as the output voltage waveform is developed using the GA and EPA algorithms. For the initial phase, the first GA algorithm is used, and the algorithm EPA is appended to the existing one to improve convergence. For three-phase inverters, differential evolution (DE) is created to improve the output voltage level [41]. To optimize the harmonic profile and eliminate low-order harmonics, DE is also utilized to determine the switching angle.

Jian et al., [42] suggest a single-phase DSTATCOM based on an S4L inverter that performs better than DSTATCOMs based on two-level inverters and three-level inverters underneath both nonlinear and linear load circumstances. The suggested inverter features a two-stage design. Three separate voltage levels of one-third, two-thirds, and full of the DC-link voltage are produced by the first stage. In the second stage, the two-level inverter receives these voltage levels. The suggested inverter output can have four levels in addition to the zero voltage that the two-level inverter generates. The DSTATCOM with S4L inverter-based outperforms conventional ones while using the same switching frequency and computation time. Model predictive control (MPC) is used to improve its performance.

Space vector control

Alternatives to the SHE approaches for MLI have been published, and they are founded on the notion of space vectors. The term "space vector control" also refers to nearest vector control [43]. It is capable of running at any low switching frequency. SHE ensures that the mean value of the necessary load voltage is not built during each time interval of switching, in contrast to space vector modulation. The NVC control's primary goal is to choose the vector that is nearest to the reference vector while minimizing the distance or space error between them.

Fixed-time step control scheme for a staircase

The staircase with a static period reign approach is castoff to construct the output voltage waveform, utilizing constant time steps at each level. Its main advantage is the simplicity of the construction and that made controlling the inverter very simple. The main disadvantage here is that lower-order harmonics dominate the output voltage profile, which raises THD. To identify equal switching instants, corresponding to the level count, the waveform is separated within equal time segments. The output voltage cannot be changed under this control method, but the input voltage of the inverter can.

Pulse width modulation

To manage the flow of power in the circuit, power electronic controlled switches are often worked in one of two modes, such as turned-off and turned-on. The switching process in operation is known as modulation. The reference-based and carrier-based PWM are the two main types of PWM approaches, and each is described here.

Reference-based pulse width modulation

There are several types of PWM techniques, including staircase modulation, trapezoidal, 60-degree, third harmonic injection, and discontinuous reference PWM. Depending on the MLI's structure, the reference signal may be unipolar or bipolar [44]. When considering a closed-loop system, the modulation signal should typically be a compensatory signal for an open-loop system, using a sinusoidal reference.

The frequency of the reference signal is fr, and the carrier switching frequency is fc. The ratio of fc/fr can be used to define the frequency modulation index [45]. To obtain a discrete spectrum with integer harmonic multiples, this ratio must have an integer value. The abbreviations for the carrier signal amplitudes and the reference signal, respectively, are Ac and Ar. The ratio of Ar to Ac can be used to define the amplitude modulation index. In PWM, the carrier signals and a reference signal are continually compared. To assert both RMS output voltage and the target output voltage level, the amplitude modulation index is a vital component.

Carrier-based pulse width modulation

Single carrier modulation and multiple carrier modulation are two categories of carrier-based modulation techniques.

Multiple Carrier Modulation: This method uses numerous triangular carriers to create a single modulating sinusoidal signal. The amount of utilized carriers are typical "$(n-1)$," where "n" denotes the inverter's level [32]. The two types of MC-PWM approaches are (i) level-shifted PWM and (ii) phase-shifted PWM. LS-PWM method is again subdivided into two approaches: variable and constant frequency. The various sorts of carrier arrangements that fall below the category of constant frequency technique include phase disposition [46], alternative phase opposition and disposition [47], phase opposition and disposition [48], variable amplitude, carrier overlapping, and hybrid techniques. The two different forms of carrier arrangements are bipolar and unipolar. For the "m"-level inverter, "$m-1$" carriers are needed in the bipolar technique, whereas "$(m-1)/2$" carriers are needed in the unipolar method [49].

(i) Phase Disposition (PD) Method: In general, all carrier signals have the same frequency and amplitude and are in the same phase. The initial distortion of the carrier is an important feature of a PD method's phase voltage spectrum. As a result, this approach produces very good line voltage performance. When using the PD method for asymmetric MLI, the harmonic contents decrease as the number of voltage levels rises.

Table 3 Comparison of merits and demerits of modulation techniques

Modulation scheme	Merits	Demerits
Selective harmonic elimination (SHE)	Lower-order harmonics can able to eliminate Harmonics are low Filter size is reduced Suitable for high-power application Efficiency is high Minimum losses during switching operation Steady-state response is better	Slower dynamic response Voltage balancing is ineffective Passive filters requirement is more
State vector control (SVC)	Effectively works at low switching frequencies Easy technique High efficiency with low harmonics Switching states are less Lesser d*v*/d*t* stress Dynamic response is good Huge passive filters not required	Lower harmonics are not eliminated Complex structure
Phase-shifted PWM (PS-PWM)	Structure is simple and modular Switching pattern rotation is not necessary	Harmonic content is high Voltage balancing is weak Dynamic response is poor
Phase disposition PWM (PD-PWM)	Voltage profile is best Optimal switching angle is achieved	Power distribution is uneven Dynamic response is poor

(ii) Phase Opposition Disposition (POD) Method: While the segments of negative carrier signals are over turning out of phase with this modulation approach, the integrant of positive carrier signals is in phase.
(iii) Alternative Phase Opposition Disposition (APOD) Technique: All carriers need to be 180 degrees out of phase with the closest carriers to apply this strategy.
(iv) Carrier Overlapping: All carrier waves overlap on one other.
(v) Variable amplitude: In this method, all carrier signals have different amplitude to one other.

The configuration of carriers depends on how much freedom is needed to produce the desired output voltage level meant for overlapping of a carrier, amplitude adjustment, and adjustable frequency approaches. Other signal types, including ramp signals, unilateral sine carriers, altered triangular carriers, and others, are also employed as carrier signals in place of conventional triangle carriers [50]. The carrier type and frequency range have a significant impact on MLI losses. The comparison of different modulation techniques, its merits and demerits are mentioned in Table 3.

Conclusion

Global advancements in various industries and academic research have resulted in a growing demand for high-energy-based efficiency converters. MLIs are highly sought after to perform a crucial part in DC/AC conversion processes including together high-power and high-voltage approaches due to their built-in advantages. The way to interact straight to intermediate voltage, a decrease in semiconductor devices, DC sources, and their related gate driver circuits, as well as improved efficiency, reduced price, and compact size are a few of the significant attributes that have propelled RSC-MLIs from

a theoretical notion to practical applications. Frequent topologies and modulation techniques are examined in this literature review, and their performance metrics are compared, and it is observed that asymmetrical multilevel inverters are superior to symmetric MLIs in terms of benefits. The main focus of the review article has primarily been on reduced switch multilevel inverter topologies. This article has a thorough discussion of the modulation strategies for both low and high switching frequencies. This review looks forward to obtain the majority of the relevant data for working in this field, including details on choosing the finest topology for a certain application, switching strategies, and control approaches.

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I/We hereby declare that this submission is entirely my work, in my own words, and that all sources used in researching it are fully acknowledged and all quotations properly identified.

Author contributions
Conceptualization was done by NVVK and TGM; validation was done by NVVK and TGM; formal analysis was done by NVVK; investigation was done by NVVK; resources were done by NVVK; data curation was done by NVVK; writing—original draft preparation were done by NVVK; writing—review and editing were done by TGM; supervision was done by TGM. NVVK and TGM participated in its design and coordination and helped to draft the manuscript. Both authors have read and agreed to the published version of the manuscript and approved the final manuscript.

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Declarations

Competing interests
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